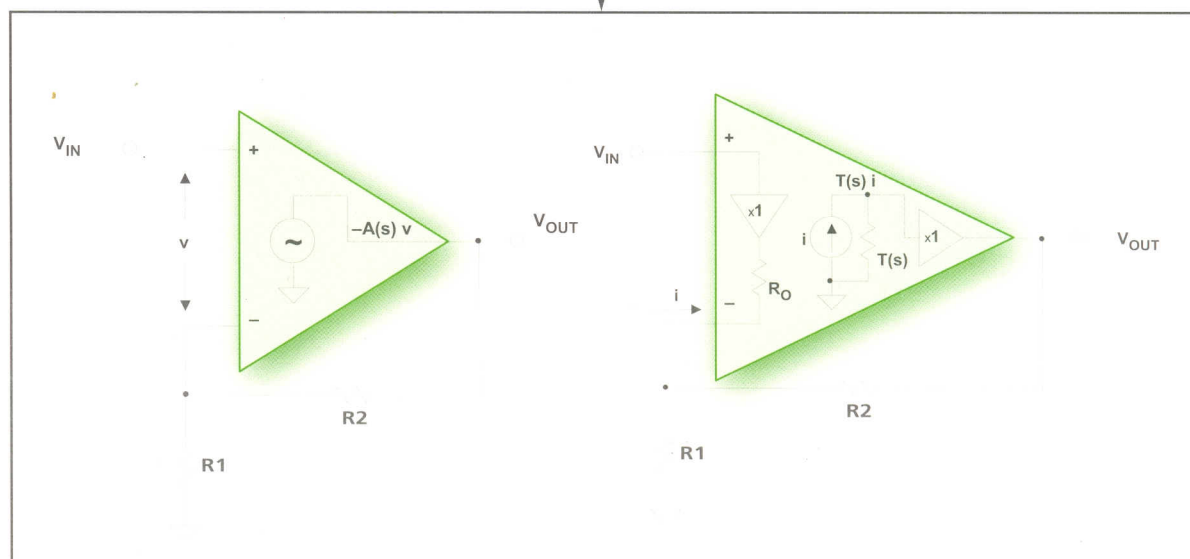
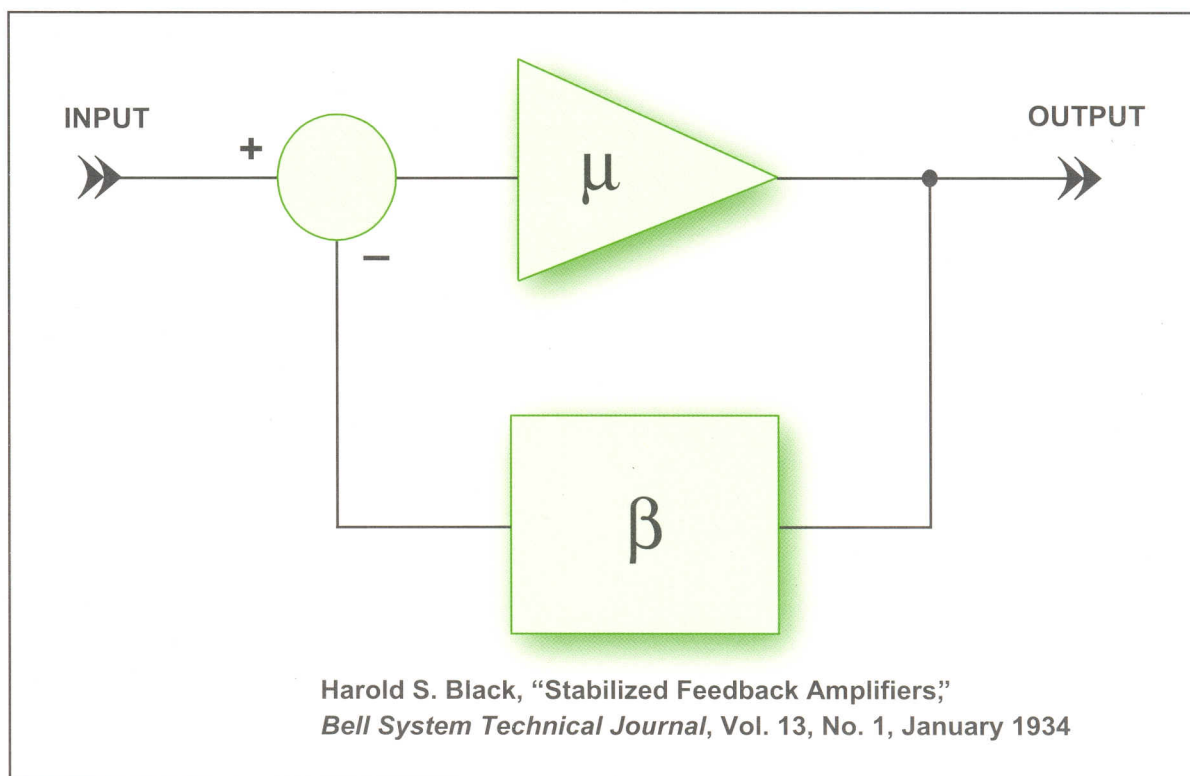
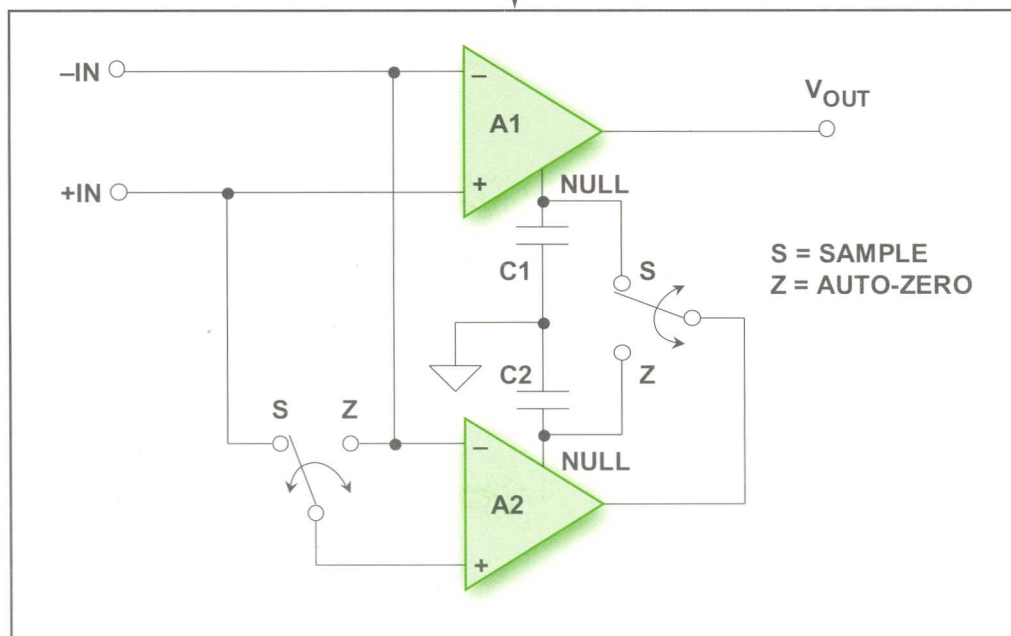
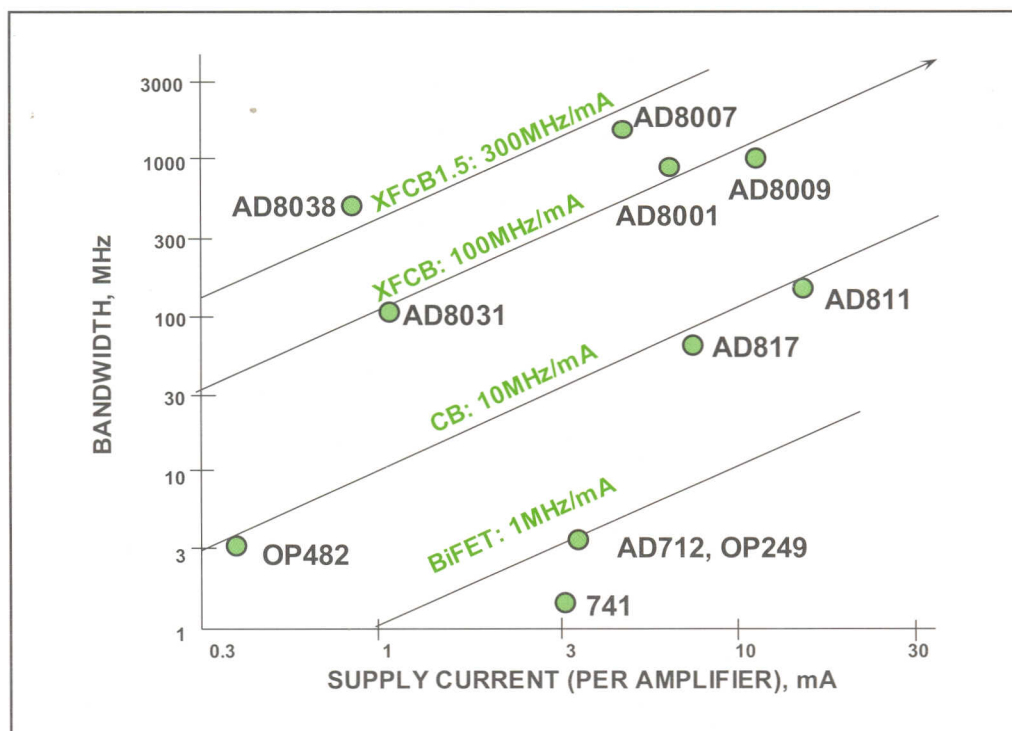


Op Amp Applications Seminar





Worldwide Headquarters
 One Technology Way
 P.O. Box 9106
 Norwood, MA
 02062-9106 U.S.A.
 Tel: 781 329 4700,
 (1 800 262 5643,
 U.S.A. only)
 Fax: 781 326 8703

Japan Headquarters
 New Pier Takeshiba
 South Tower Building
 1-16-1 Kaigan,
 Minato-ku, Tokyo
 105-6891, Japan
 Tel: 813 5402 8200
 Fax: 813 5402 1063

Southeast Asia Headquarters
 4501 Nat West Tower
 Times Square
 1 Matheson Street
 Causeway Bay
 Hong Kong, PRC
 Tel: 852 2 506 9336
 Fax: 852 2 506 4755

Many of the figures presented in this seminar book have been extracted from the following Analog Devices publication:

OP AMP APPLICATIONS SEMINAR

A reference to the appropriate chapters in this book is given underneath the slides in this book where appropriate.



© Analog Devices, Inc., 2002
All Rights Reserved

Many of the figures presented in this seminar book have been extracted from the following Analog Devices publication:

Op Amp Applications

Walter G. Jung
Analog Devices, 2002

A reference to the appropriate chapters in the above book is given underneath the slides in this book where appropriate.



© Analog Devices, Inc., 2002
All Rights Reserved

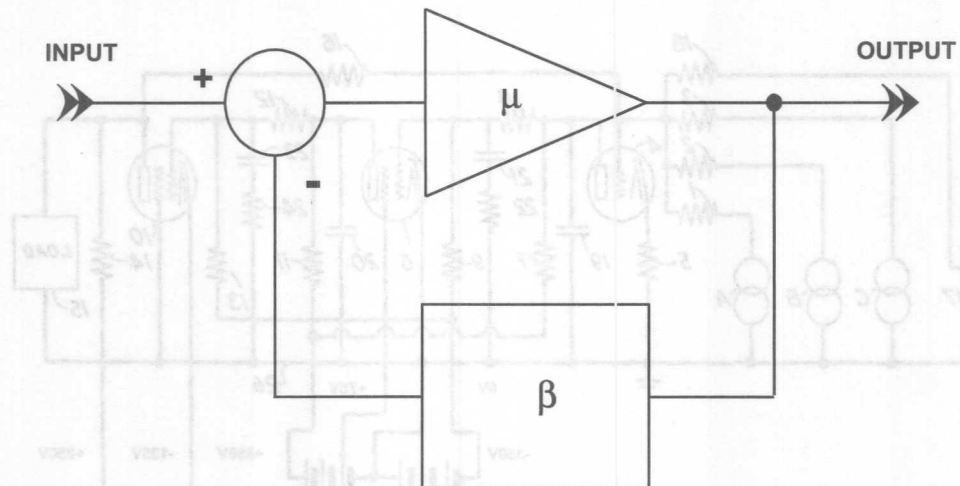
OP AMP APPLICATIONS SEMINAR

- 1. History, Basics, Design Aids, Filters**
2. Specialty Amplifiers, Using Op Amps with Data Converters
3. Hardware and Housekeeping Design Techniques
4. Signal Amplifiers, Sensor Signal Conditioning

OP AMP APPLICATIONS SEMINAR

1. History, Basics, Design Aids, Filters
2. Specialty Amplifiers, Using Op Amps with Data Converters
3. Hardware and Housekeeping Design Techniques
4. Signal Amplifiers, Sensor Signal Conditioning

HAROLD BLACK'S FEEDBACK AMPLIFIER



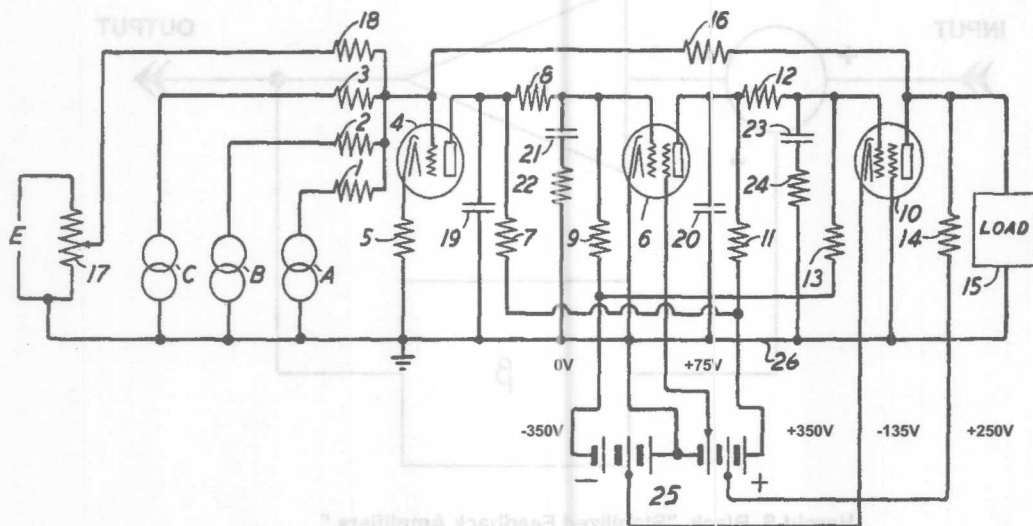
Harold S. Black, "Stabilized Feedback Amplifiers,"
Bell System Technical Journal, Vol. 13, No. 1, January 1934

Op Amp Applications, Chapter H

1.1

■ OP AMP APPLICATIONS SEMINAR

SCHEMATIC DIAGRAM FOR "SUMMING AMPLIFIER" (US PATENT 2,401,779, ASSIGNED TO BELL TELEPHONE LABORATORIES, INC.)

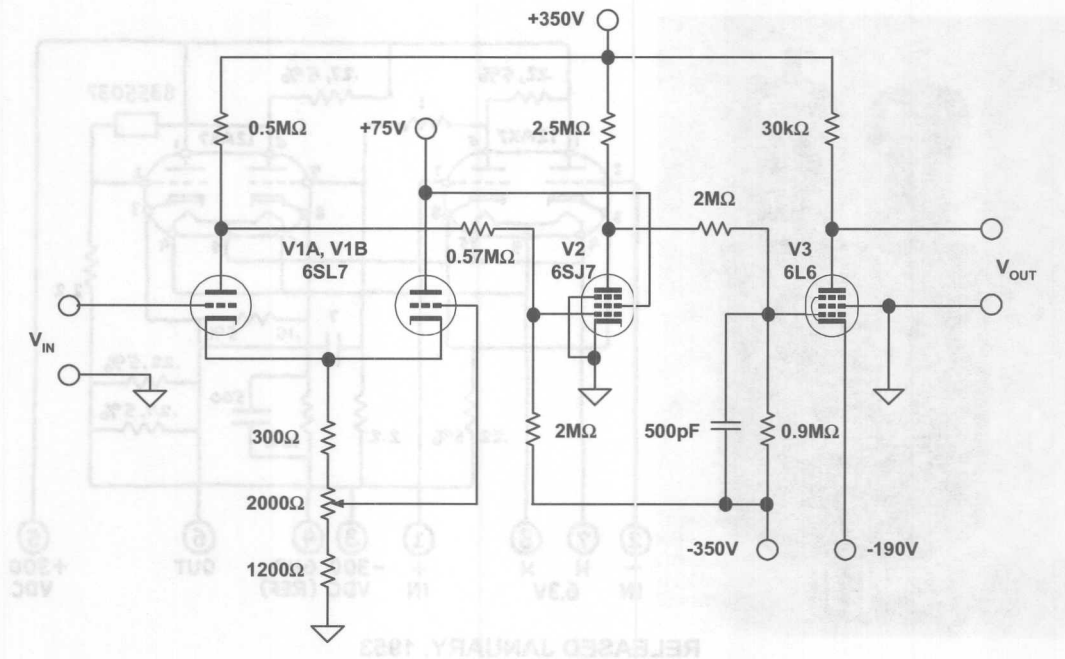


K. D. Swartzel, Jr., "Summing Amplifier," US Patent 2,401,779,
filed May 1, 1941, issued July 11, 1946

Op Amp Applications, Chapter H

1.2

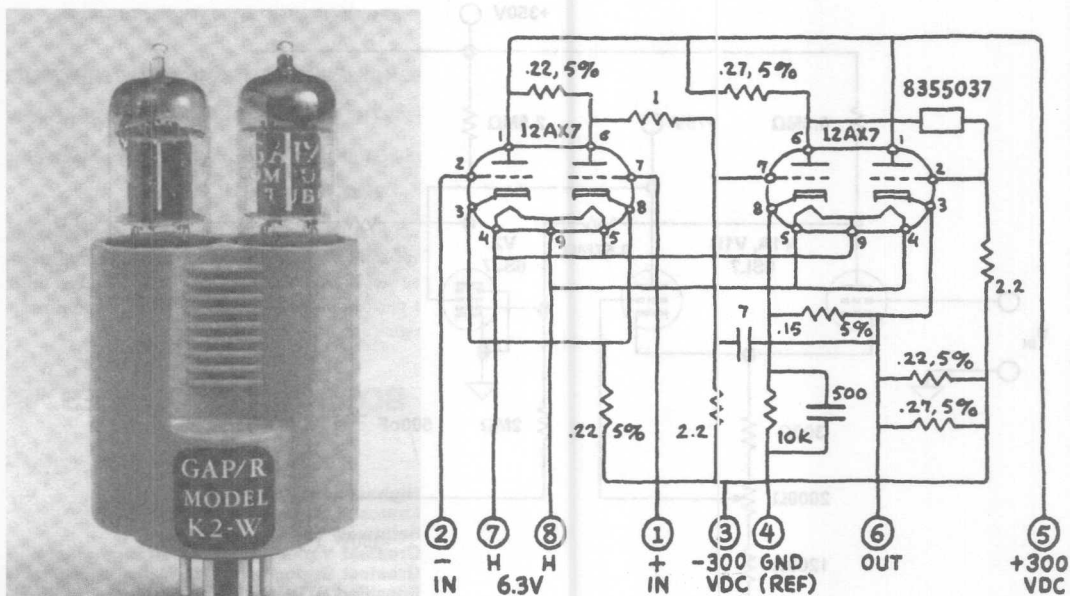
**SCHEMATIC DIAGRAM OF LATE M9 SYSTEM OP AMP DESIGNED AT
BELL TELEPHONE LABORATORIES (1941-1945)**



Op Amp Applications, Chapter H

1.3

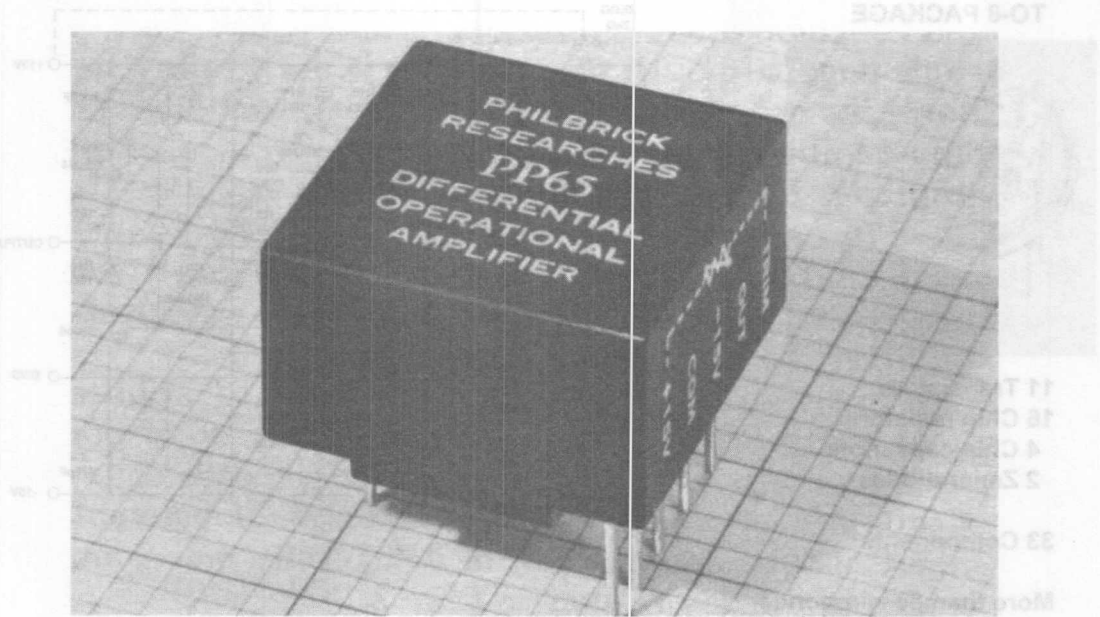
THE GAP/R K2-W OP AMP, PHOTO AND SCHEMATIC DIAGRAM
(COURTESY OF GAP/R ALUMNUS DAN SHEINGOLD)



Op Amp Applications, Chapter H

1.4

THE GAP/R MODEL PP65 POTTED MODULE SOLID-STATE OP AMP (1962)

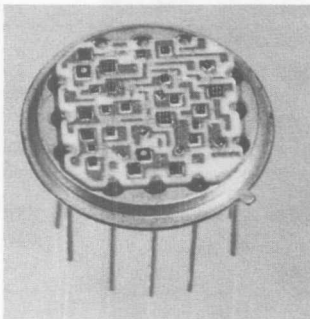


Op Amp Applications, Chapter H

Op Amp Applications, Chapter H 1.5

THE ADI HOS-050 HIGH SPEED HYBRID IC OP AMP PHOTO AND SCHEMATIC DIAGRAM (1977)

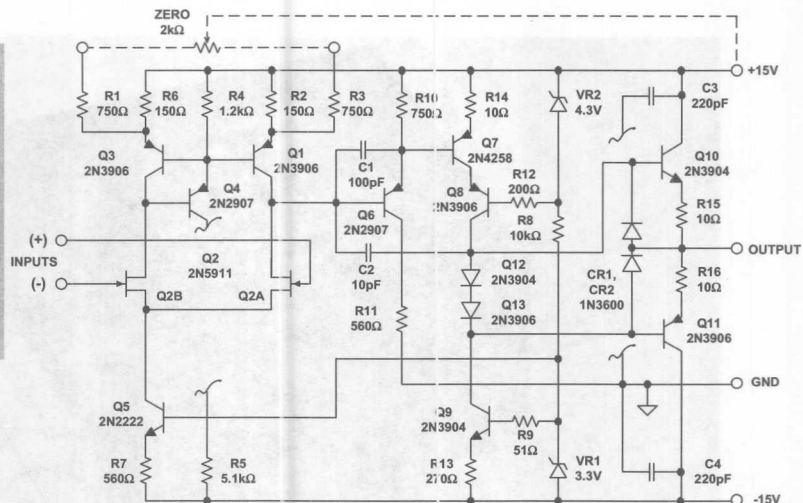
TO-8 PACKAGE



11 Transistors
16 Chip resistors
4 Chip capacitors
2 Zener diodes

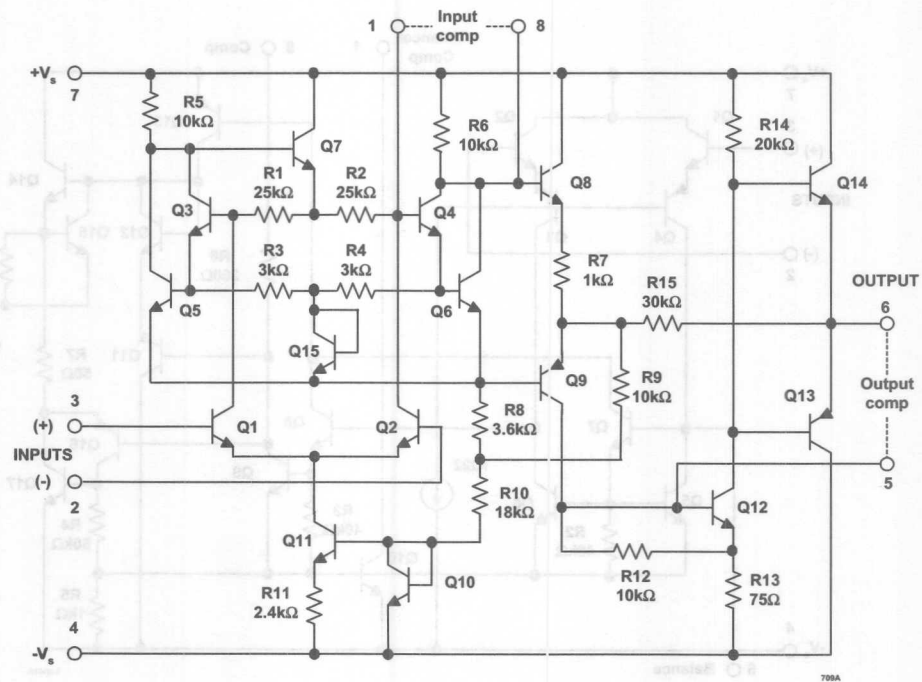
33 Components

More than 60 wirebonds



Op Amp Applications, Chapter H

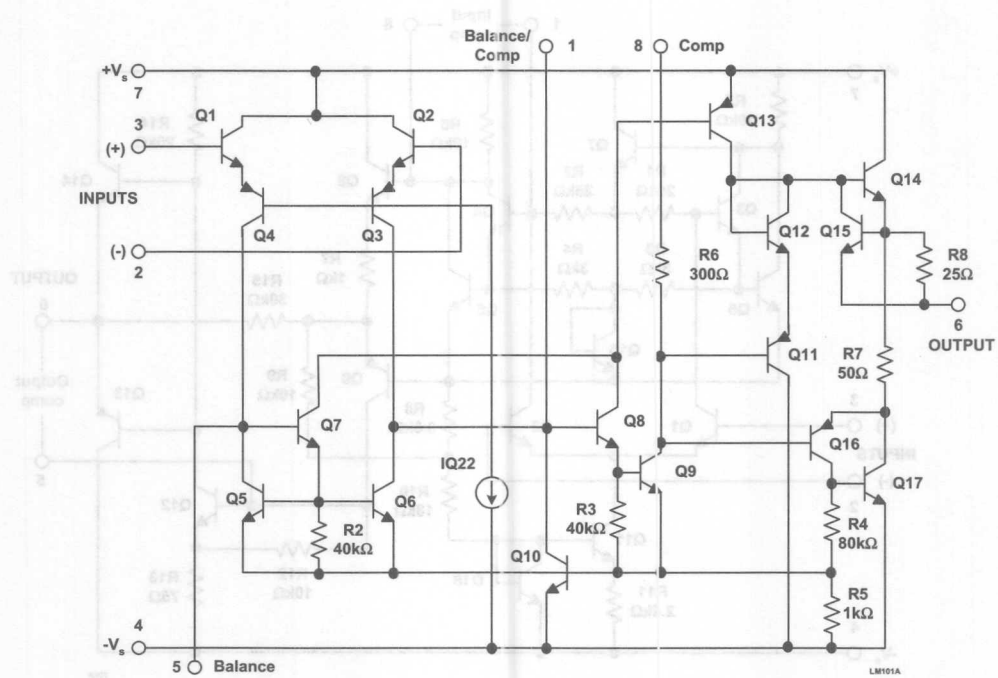
1.6

THE μ A709 MONOLITHIC IC OP AMP (1965)

Op Amp Applications, Chapter H

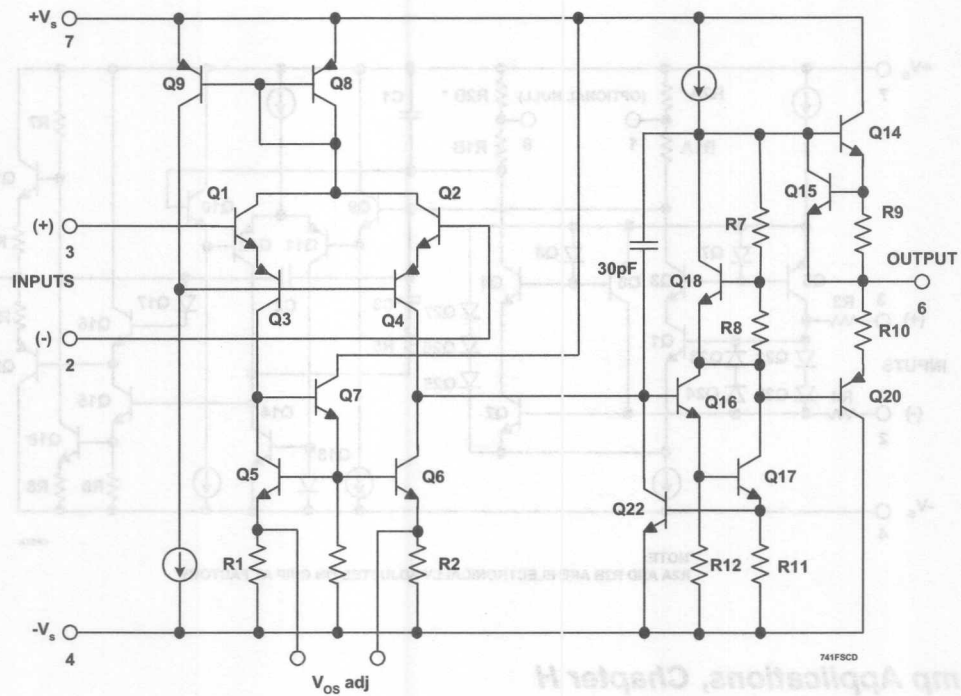
1.7

THE LM101 MONOLITHIC IC OP AMP (1967)



Op Amp Applications, Chapter H

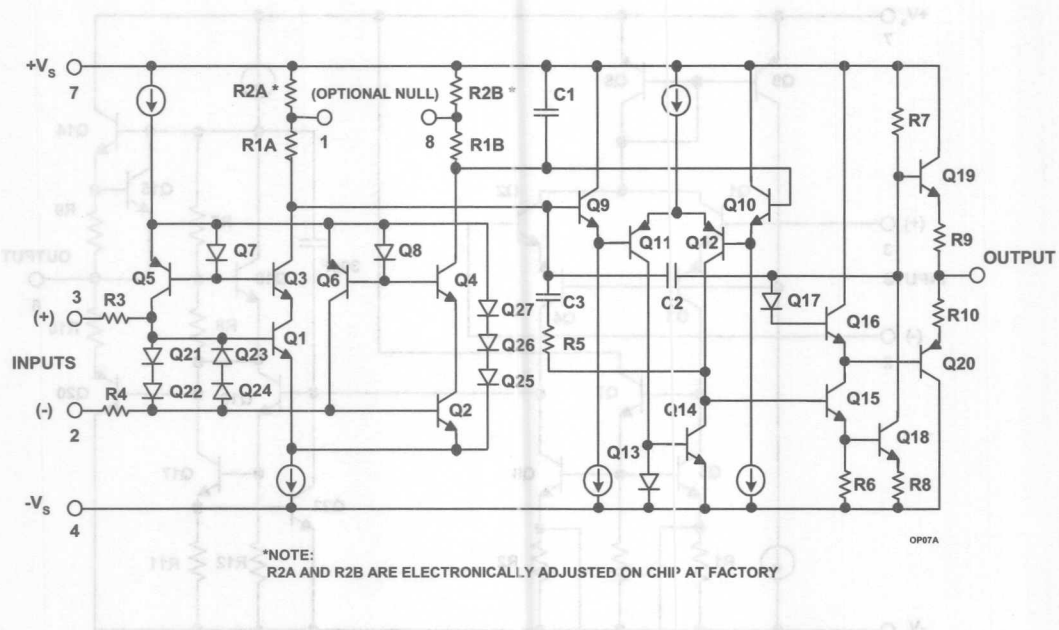
1.8

THE μ A741 MONOLITHIC IC OP AMP (1968)

Op Amp Applications, Chapter H

1.9

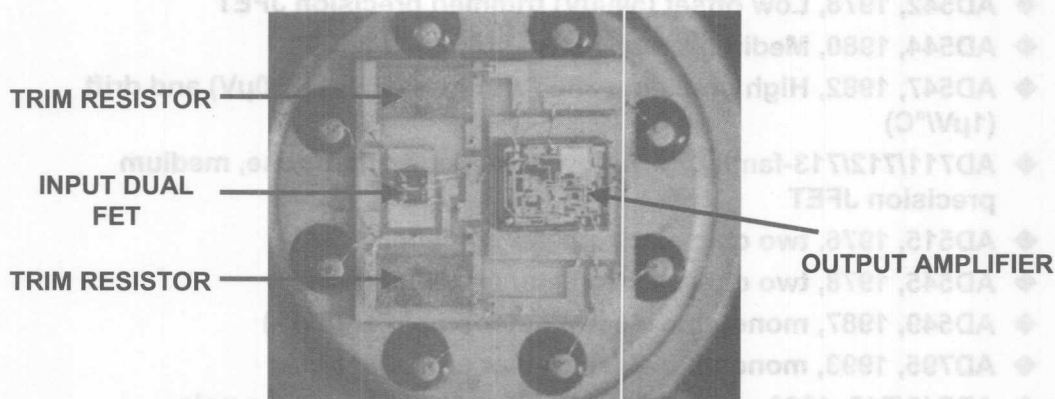
THE OP07 MONOLITHIC IC OP AMP (1975)



Op Amp Applications, Chapter H

1.10

THE AD503 AND AD506 TWO CHIP HYBRID IC OP AMPS (1970)



Op Amp Applications, Chapter H

1.11

KEY ADI IC FET OP AMP CHRONOLOGY

- ◆ AD542, 1978, Low offset (500 μ V) trimmed precision JFET
- ◆ AD544, 1980, Medium speed (8V/ μ s) trimmed JFET
- ◆ AD547, 1982, High precision JFET trimmed offset (250 μ V) and drift (1 μ V/ $^{\circ}$ C)
- ◆ AD711/712/713-family, 1986, low cost, general purpose, medium precision JFET
- ◆ AD515, 1976, two chip electrometer amplifier (75fA)
- ◆ AD545, 1978, two chip electrometer amplifier (1pA)
- ◆ AD549, 1987, monolithic electrometer amplifier (60fA)
- ◆ AD795, 1993, monolithic electrometer amplifier (1pA)
- ◆ AD743/745, 1990, monolithic JFETS, 1.9nV/ $\sqrt{\text{Hz}}$ voltage noise
- ◆ AD820/822/824, 1993, JFETs, single-supply, rail-to-rail output (3 to 36V supply)
- ◆ AD823, 1995, JFET, single-supply, rail-to-rail output (3 to 36V supply), high speed
- ◆ AD8610/8620, 2002, precision, low noise, high speed JFET
- ◆ AD8065/8066/8067, AD8033/8034, 2002, high speed FastFET™

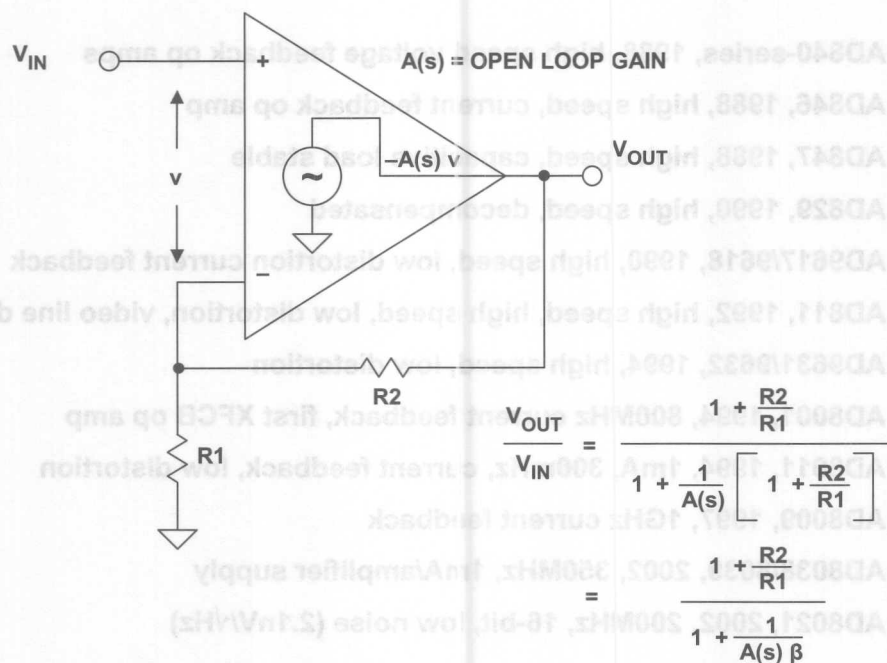
KEY ADI HIGH SPEED COMPLEMENTARY BIPOLAR OP AMPS

- ◆ AD840-series, 1988, high speed voltage feedback op amps
- ◆ AD846, 1988, high speed, current feedback op amp
- ◆ AD847, 1988, high speed, capacitive load stable
- ◆ AD829, 1990, high speed, decompensated
- ◆ AD9617/9618, 1990, high speed, low distortion current feedback
- ◆ AD811, 1992, high speed, high speed, low distortion, video line driver
- ◆ AD9631/9632, 1994, high speed, low distortion
- ◆ AD8001, 1994, 800MHz current feedback, first XFCEB op amp
- ◆ AD8011, 1994, 1mA, 300MHz, current feedback, low distortion
- ◆ AD8009, 1997, 1GHz current feedback
- ◆ AD8038/8039, 2002, 350MHz, 1mA/amplifier supply
- ◆ AD8021, 2002, 200MHz, 16-bit, low noise (2.1nV/√Hz)

Op Amp Applications, Chapter H

1.13

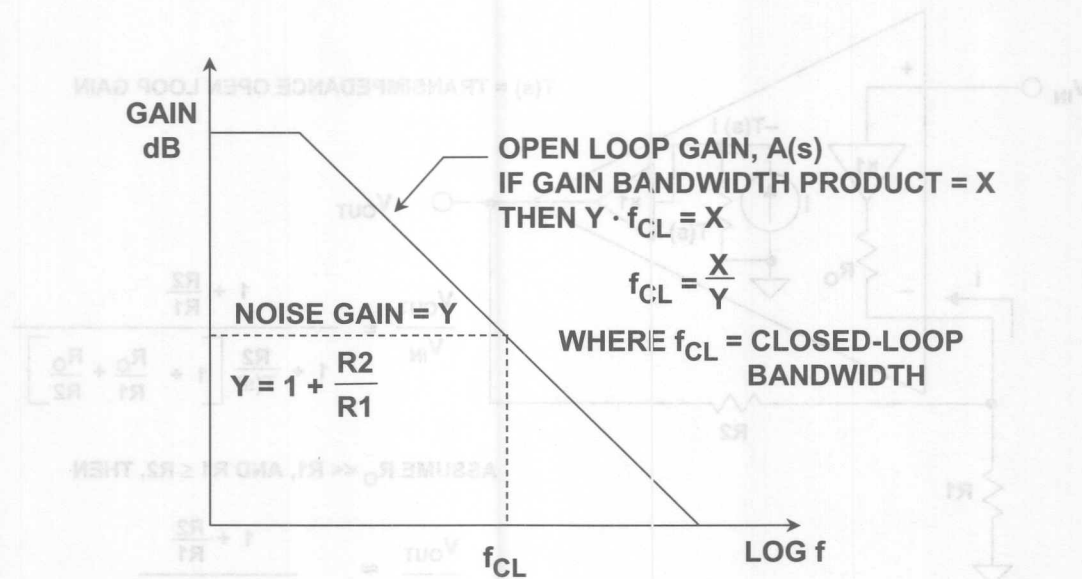
VOLTAGE FEEDBACK (VFB) OP AMP MODEL



Op Amp Applications, Chapter 1

1.14

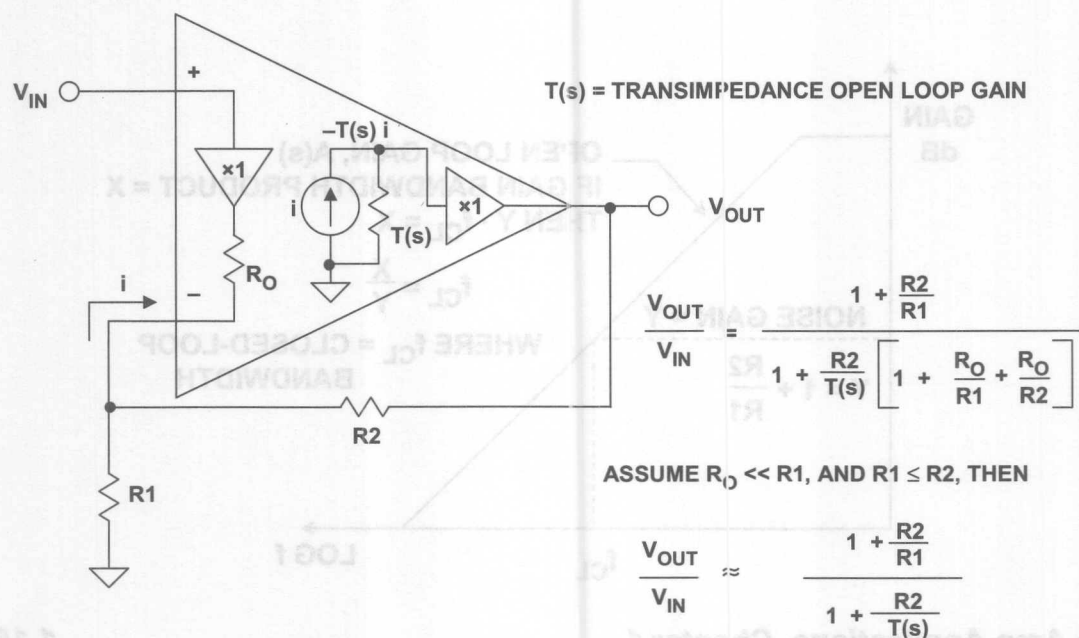
GAIN-BANDWIDTH PRODUCT FOR VOLTAGE FEEDBACK OP AMPS



Op Amp Applications, Chapter 1

1.15

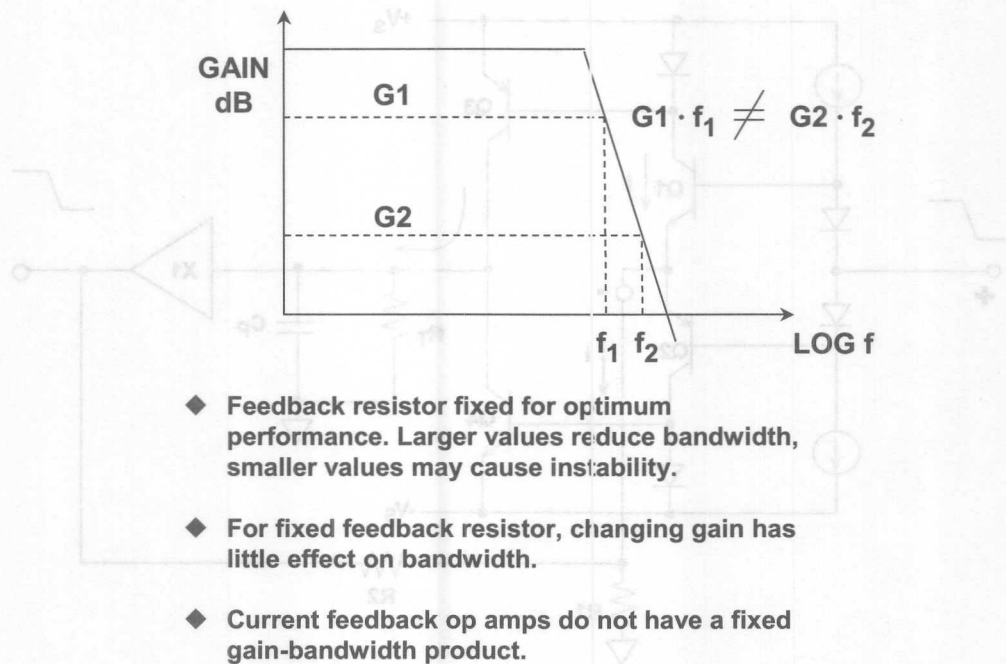
CURRENT FEEDBACK (CFB) OP AMP MODEL



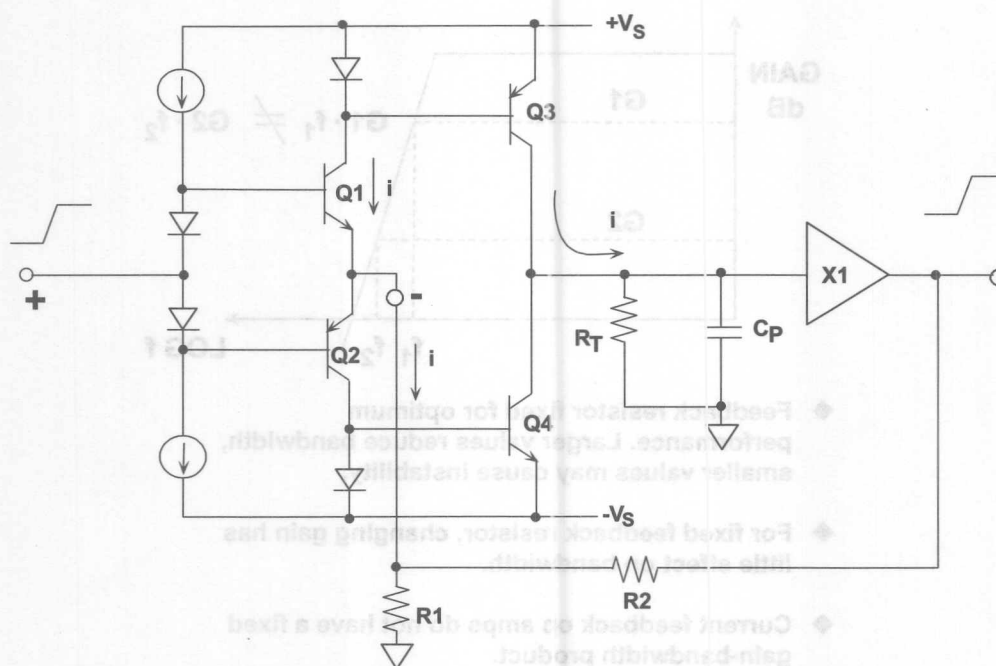
Op Amp Applications, Chapter 1

1.16

FREQUENCY RESPONSE FOR CURRENT FEEDBACK OP AMPS



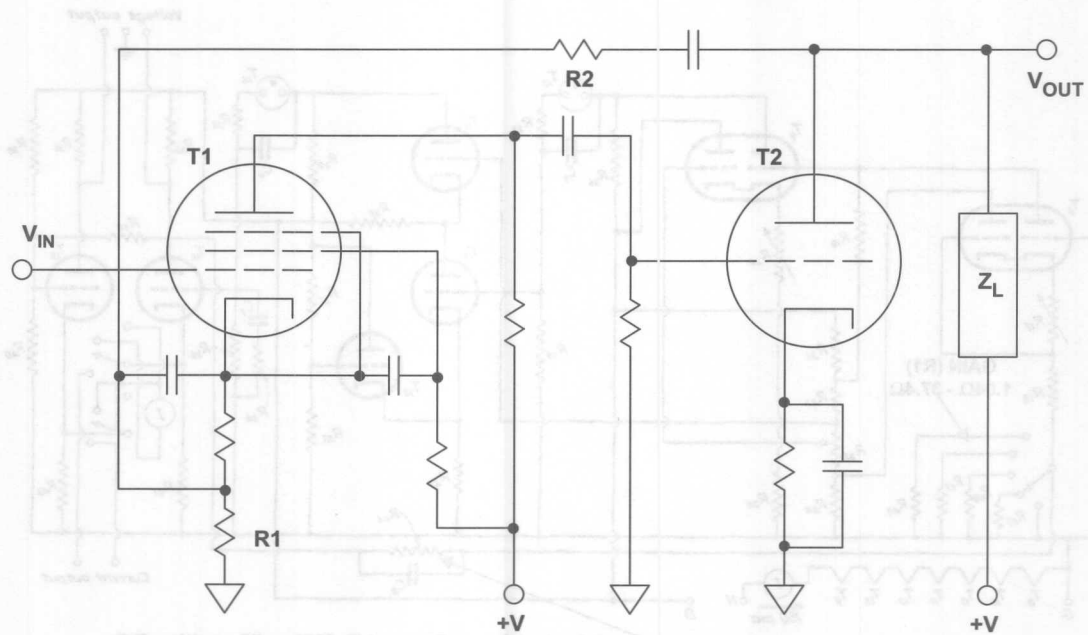
SIMPLIFIED CURRENT FEEDBACK (CFB) OP AMP



Op Amp Applications, Chapter 1

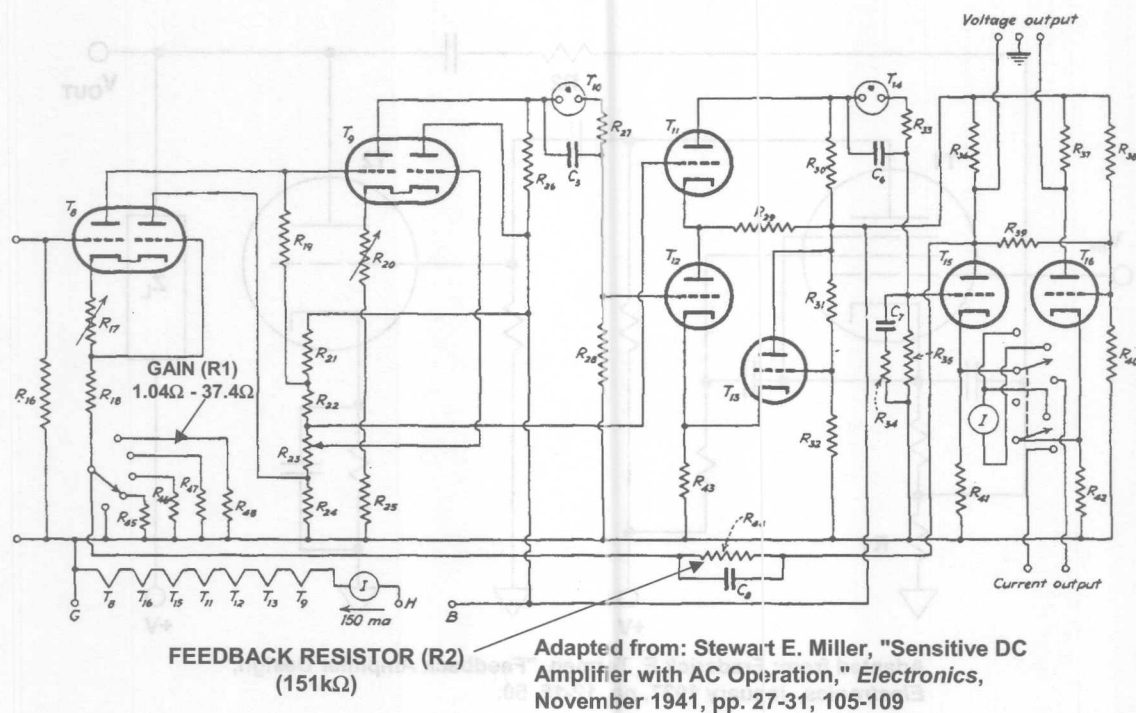
1.18

**A 1937 VACUUM TUBE AMPLIFIER DESIGNED BY FREDERICK E. TERMAN USING
CURRENT FEEDBACK TO THE LOW IMPEDANCE INPUT CATHODE**



Adapted from: Frederick E. Terman, "Feedback Amplifier Design,"
Electronics, January 1937, pp. 12-15, 50.

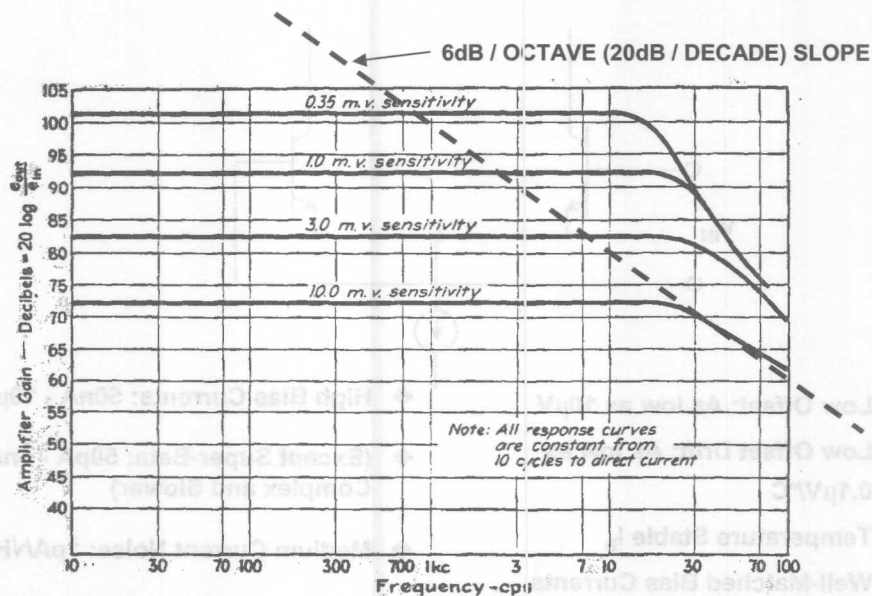
A 1941 VACUUM TUBE AMPLIFIER WITH CURRENT FEEDBACK



Op Amp Applications, Chapter 1

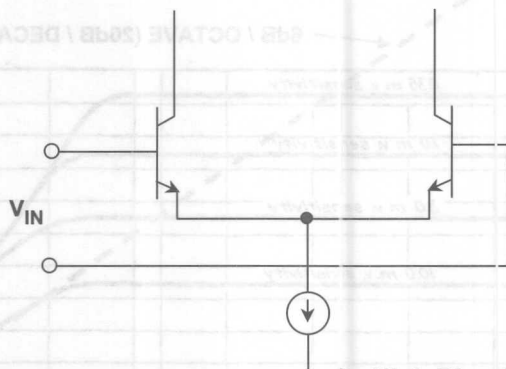
1.20

A 1941 CIRCUIT SHOWS CHARACTERISTIC CFB GAIN - BANDWIDTH RELATIONSHIP



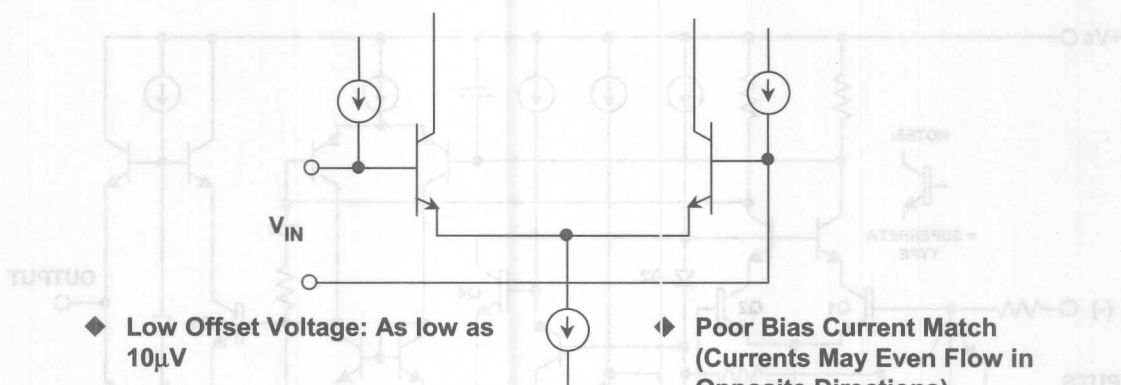
Adapted from: Stewart E. Miller, "Sensitive DC Amplifier with AC Operation,"
Electronics, November 1941, pp. 27-31, 105-109

BIPOLAR TRANSISTOR INPUT STAGE



- ◆ Low Offset: As low as $10\mu\text{V}$
- ◆ Low Offset Drift: As low as $0.1\mu\text{V}/^\circ\text{C}$
- ◆ Temperature Stable I_B
- ◆ Well-Matched Bias Currents
- ◆ Low Voltage Noise: As low as $1\text{nV}/\sqrt{\text{Hz}}$
- ◆ High Bias Currents: $50\text{nA} - 10\mu\text{A}$
- ◆ (Except Super-Beta: $50\text{pA} - 5\text{nA}$, More Complex and Slower)
- ◆ Medium Current Noise: $1\text{pA}/\sqrt{\text{Hz}}$
- ◆ Matching source impedances minimize offset error due to bias current

BIAS-CURRENT COMPENSATED BIPOLAR INPUT STAGE

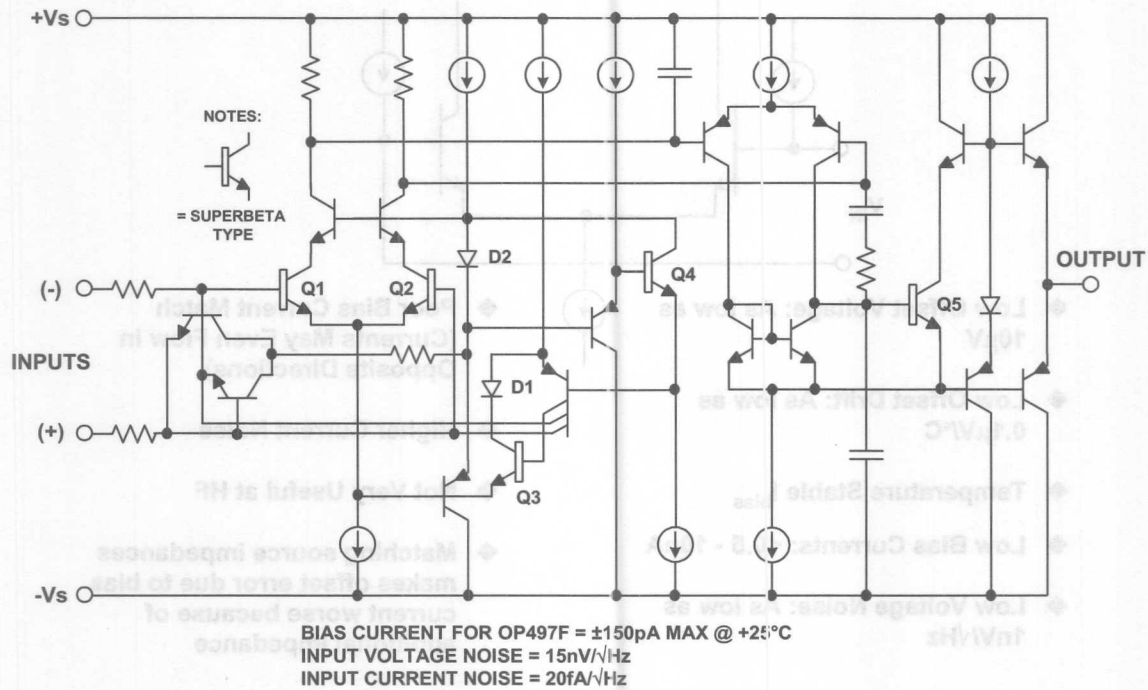


- ◆ Low Offset Voltage: As low as $10\mu\text{V}$
- ◆ Low Offset Drift: As low as $0.1\mu\text{V}/^\circ\text{C}$
- ◆ Temperature Stable I_{bias}
- ◆ Low Bias Currents: $<0.5 - 10\text{nA}$
- ◆ Low Voltage Noise: As low as $1\text{nV}/\sqrt{\text{Hz}}$
- ◆ Poor Bias Current Match (Currents May Even Flow in Opposite Directions)
- ◆ Higher Current Noise
- ◆ Not Very Useful at HF
- ◆ Matching source impedances makes offset error due to bias current worse because of additional impedance

Op Amp Applications, Chapter 1

1.23

OP497 OP AMP USES SUPER-BETA TRANSISTORS AND BIAS CURRENT COMPENSATION



SINGLE-SUPPLY OP AMPS

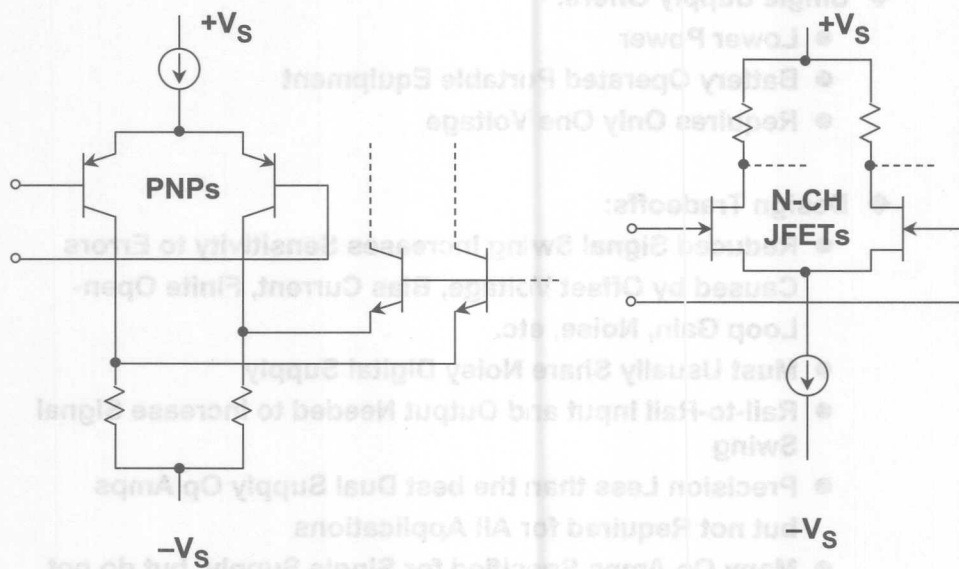
◆ **Single Supply Offers:**

- Lower Power
- Battery Operated Portable Equipment
- Requires Only One Voltage

◆ **Design Tradeoffs:**

- Reduced Signal Swing Increases Sensitivity to Errors Caused by Offset Voltage, Bias Current, Finite Open-Loop Gain, Noise, etc.
- Must Usually Share Noisy Digital Supply
- Rail-to-Rail Input and Output Needed to Increase Signal Swing
- Precision Less than the best Dual Supply Op Amps but not Required for All Applications
- Many Op Amps Specified for Single Supply, but do not have Rail-to-Rail Inputs or Outputs

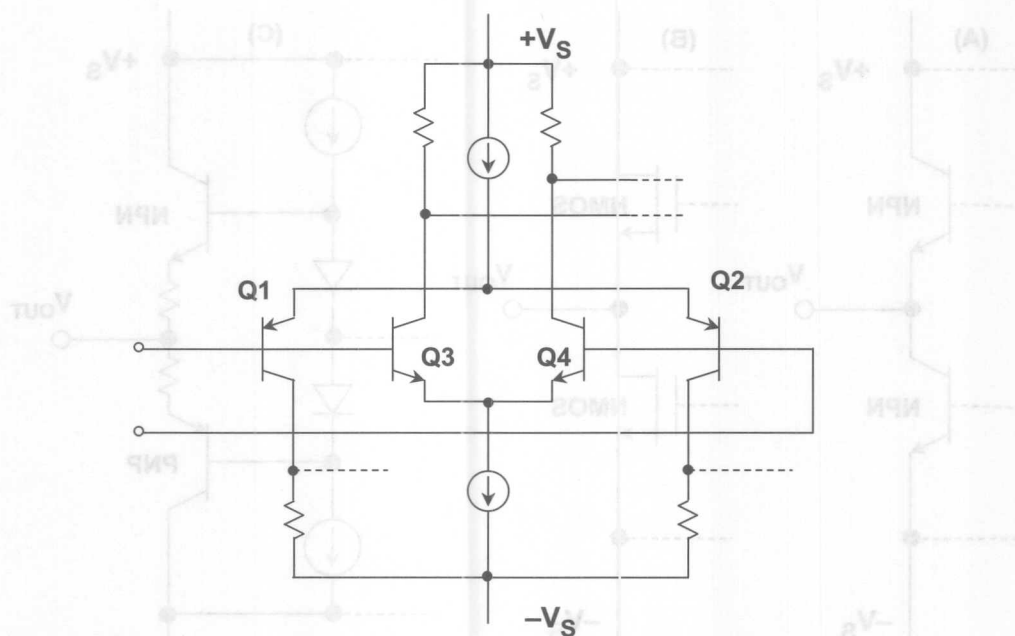
PNP OR N-CCHANNEL JFET STAGES ALLOW INPUT SIGNAL TO GO TO THE NEGATIVE RAIL



Op Amp Applications, Chapter 1

1.26

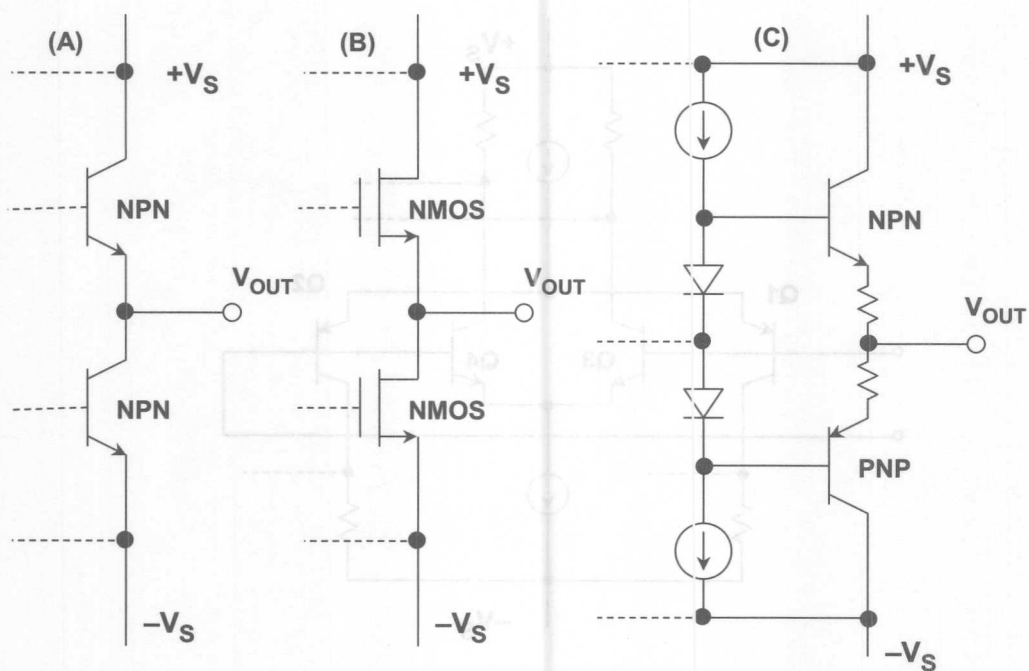
TRUE RAIL-TO-RAIL INPUT STAGE



Op Amp Applications, Chapter 1

1.27

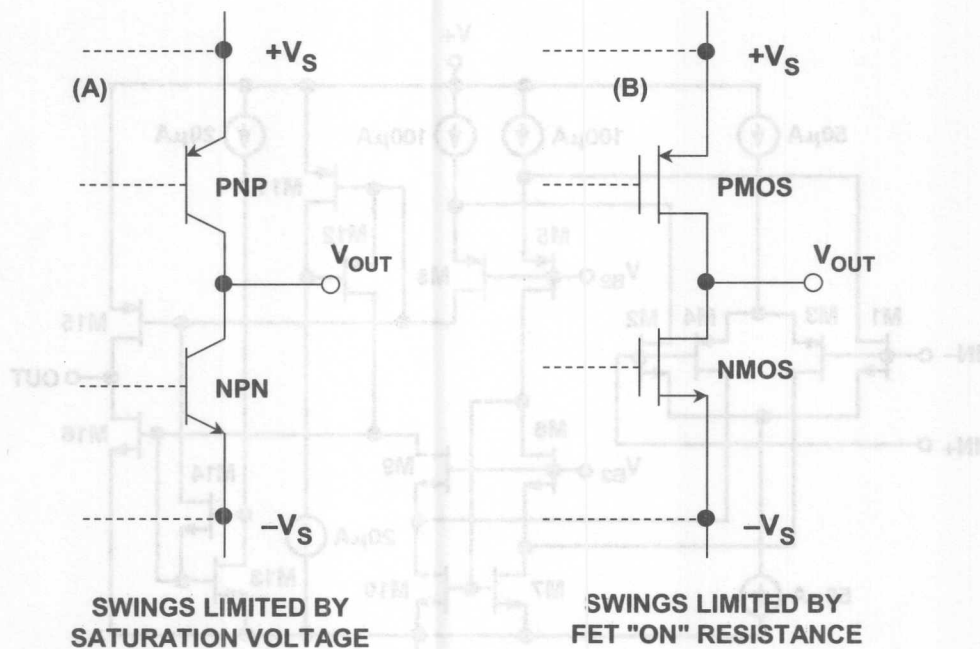
TRADITIONAL OUTPUT STAGES



Op Amp Applications, Chapter 1

1.28

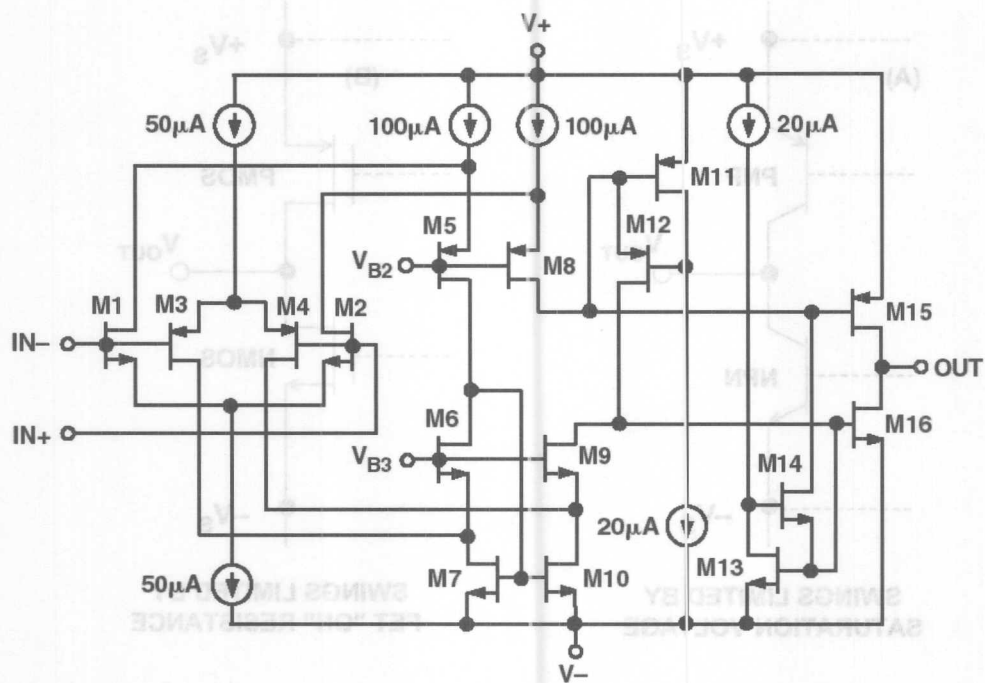
"ALMOST" RAIL-TO-RAIL OUTPUT STRUCTURES



Op Amp Applications, Chapter 1

1.29

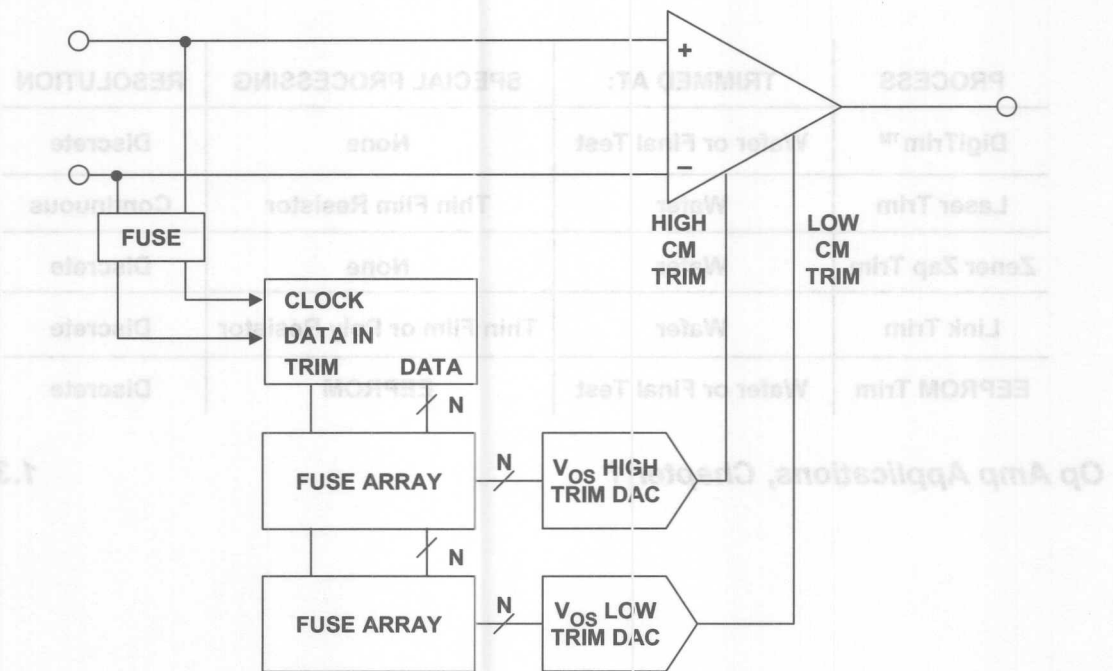
AD8531/8532/8534 CMOS RAIL-TO-RAIL OP AMP SIMPLIFIED SCHEMATIC



Op Amp Applications, Chapter 1

1.30

AD8602 (1/2) CMOS OP AMP SHOWING DigiTrim™



Op Amp Applications, Chapter 1

1.31

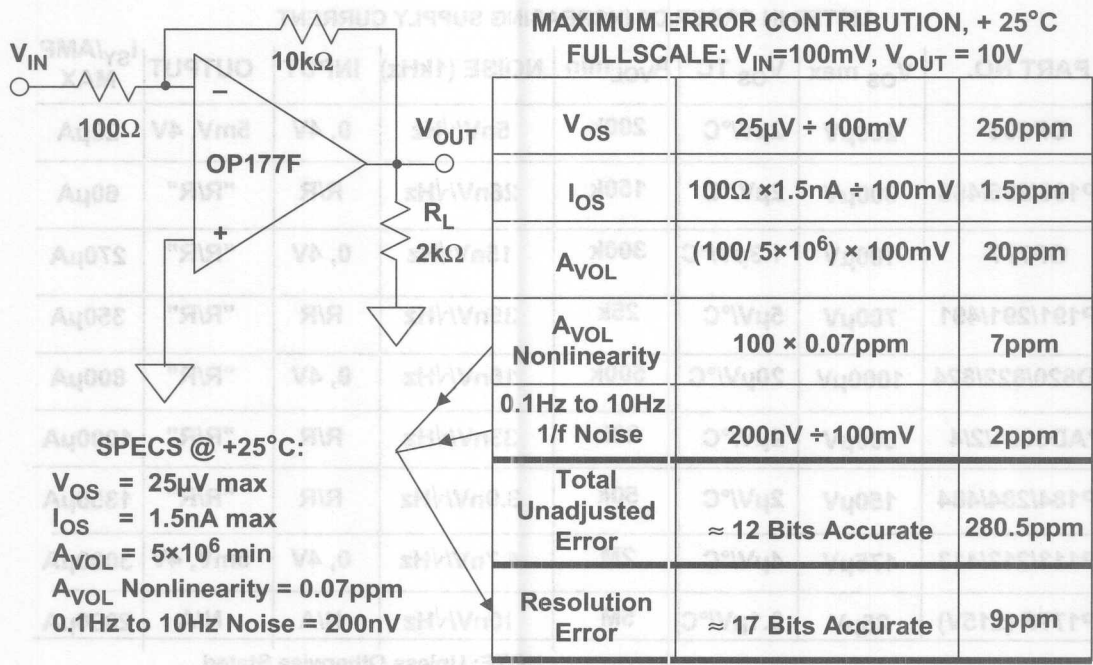
SUMMARY OF TRIM PROCESSES AT ANALOG DEVICES

PROCESS	TRIMMED AT:	SPECIAL PROCESSING	RESOLUTION
DigiTrim™	Wafer or Final Test	None	Discrete
Laser Trim	Wafer	Thin Film Resistor	Continuous
Zener Zap Trim	Wafer	None	Discrete
Link Trim	Wafer	Thin Film or Poly Resistor	Discrete
EEPROM Trim	Wafer or Final Test	EEPROM	Discrete

Op Amp Applications, Chapter 1

1.32

PRECISION OP AMP (OP177F) DC ERROR BUDGET



PRECISION SINGLE-SUPPLY OP AMP PERFORMANCE CHARACTERISTICS

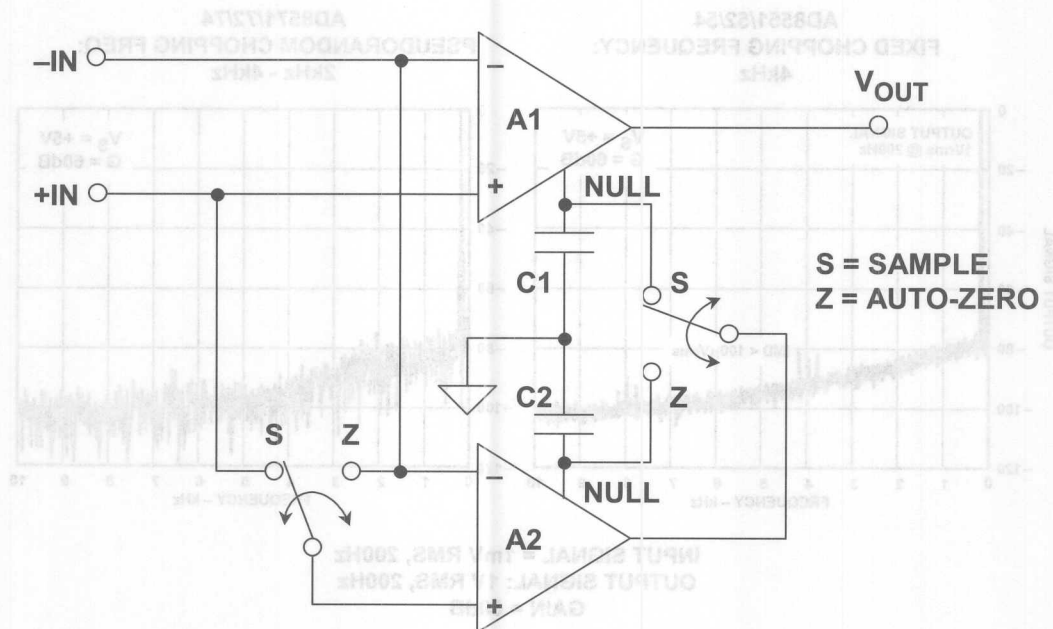
LISTED IN ORDER OF INCREASING SUPPLY CURRENT

PART NO.	V_{OS} max	V_{OS} TC	A_{VOL} min	NOISE (1kHz)	INPUT	OUTPUT	I_{SY}/AMP MAX
OP293	250 μ V	2 μ V/ $^{\circ}$ C	200k	5nV/ \sqrt{Hz}	0, 4V	5mV, 4V	20 μ A
OP196/296/496	300 μ V	2 μ V/ $^{\circ}$ C	150k	26nV/ \sqrt{Hz}	R/R	"R/R"	60 μ A
OP777	100 μ V	1.3 μ V/ $^{\circ}$ C	300k	15nV/ \sqrt{Hz}	0, 4V	"R/R"	270 μ A
OP191/291/491	700 μ V	5 μ V/ $^{\circ}$ C	25k	35nV/ \sqrt{Hz}	R/R	"R/R"	350 μ A
*AD820/822/824	1000 μ V	20 μ V/ $^{\circ}$ C	500k	16nV/ \sqrt{Hz}	0, 4V	"R/R"	800 μ A
**AD8601/2/4	600 μ V	2 μ V/ $^{\circ}$ C	20k	33nV/ \sqrt{Hz}	R/R	"R/R"	1000 μ A
OP184/284/484	150 μ V	2 μ V/ $^{\circ}$ C	50k	3.9nV/ \sqrt{Hz}	R/R	"R/R"	1350 μ A
OP113/213/413	175 μ V	4 μ V/ $^{\circ}$ C	2M	4.7nV/ \sqrt{Hz}	0, 4V	5mV, 4V	3000 μ A
OP177F (\pm 15V)	25 μ V	0.1 μ V/ $^{\circ}$ C	5M	10nV/ \sqrt{Hz}	N/A	N/A	2000 μ A

*JFET INPUT **CMOS

NOTE: Unless Otherwise Stated
Specifications are Typical @ +25 $^{\circ}$ C
 V_S = +5V

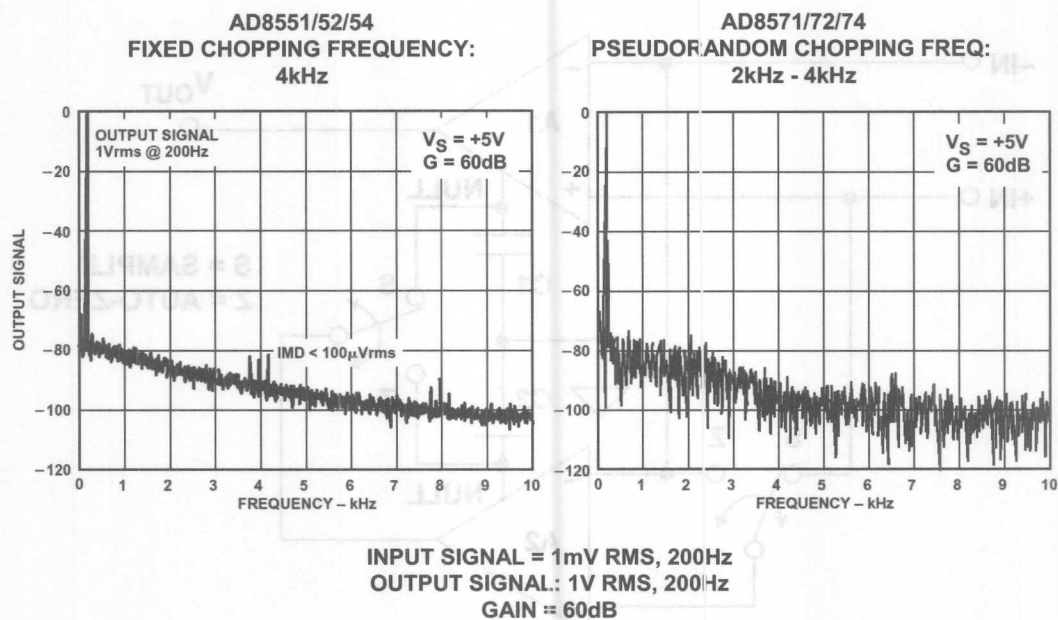
MODERN CHOPPER STABILIZED AMPLIFIER



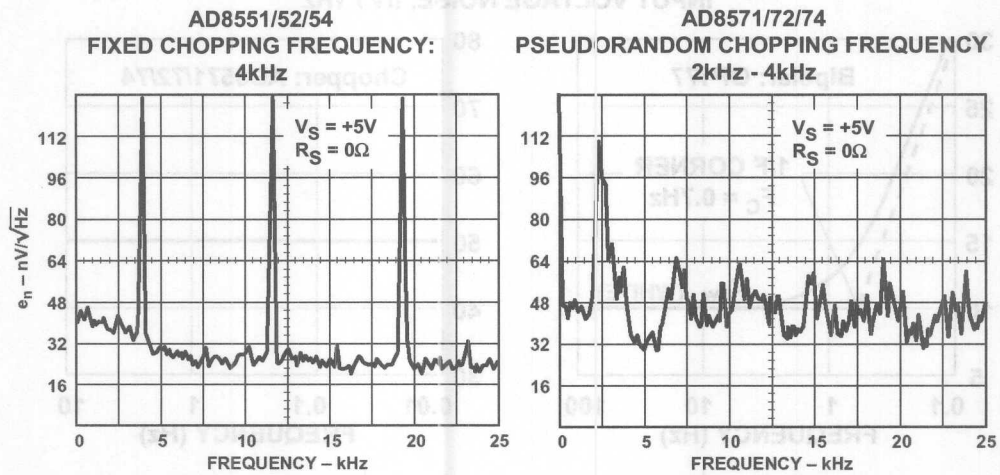
Op Amp Applications, Chapter 1

1.35

INTERMODULATION PRODUCTS: FIXED VERSUS PSEUDORANDOM CHOPPING FREQUENCY



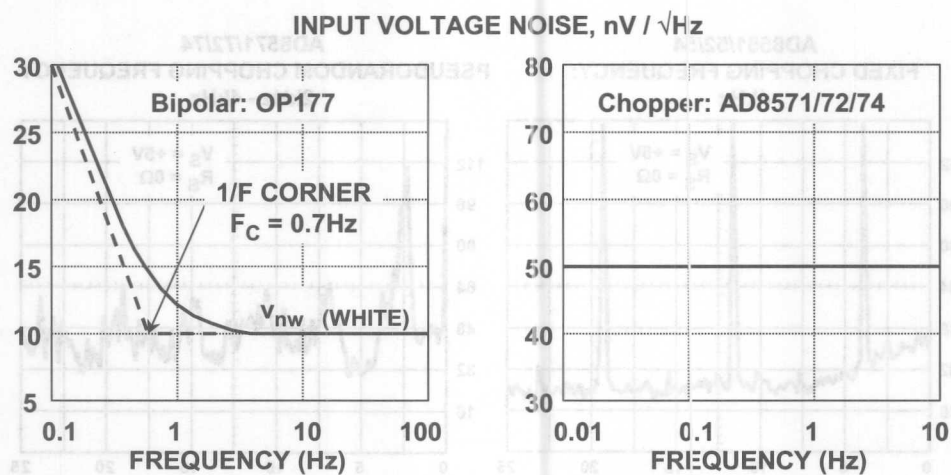
VOLTAGE NOISE SPECTRAL DENSITY COMPARISON: FIXED VERSUS PSEUDORANDOM CHOPPING FREQUENCY



Op Amp Applications, Chapter 1

1.37

NOISE: BIPOLAR VERSUS CHOPPER AMPLIFIER



NOISE BW	BIPOLAR (OP177)	CHOPPER (AD8571/72/74)
0.1Hz to 10Hz	0.238 μV p-p	1.3 μV p-p
0.01Hz to 1Hz	0.135 μV p-p	0.41 μV p-p
0.001Hz to 0.1Hz	0.120 μV p-p	0.130 μV p-p
0.0001Hz to 0.01Hz	0.118 μV p-p	0.042 μV p-p

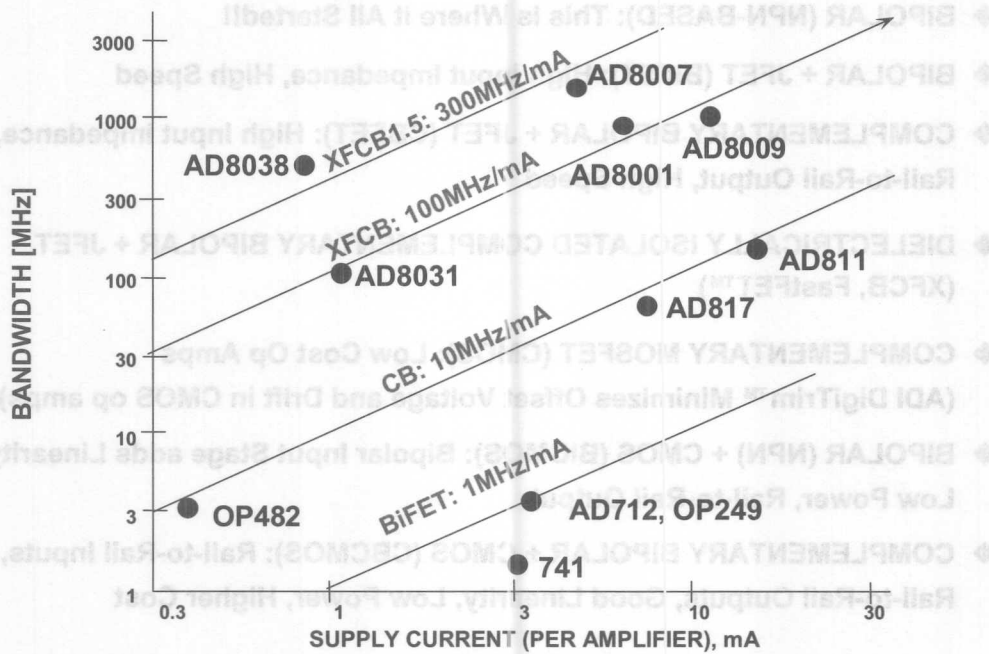
OP AMP PROCESS TECHNOLOGY SUMMARY

- ◆ **BIPOLAR (NPN-BASED):** This is Where it All Started!!
- ◆ **BIPOLAR + JFET (BiFET):** High Input Impedance, High Speed
- ◆ **COMPLEMENTARY BIPOLAR + JFET (CBiFET):** High Input Impedance, Rail-to-Rail Output, High Speed
- ◆ **DIELECTRICALLY ISOLATED COMPLEMENTARY BIPOLAR + JFET (XFCB, FastFET™)**
- ◆ **COMPLEMENTARY MOSFET (CMOS):** Low Cost Op Amps (ADI DigiTrim™ Minimizes Offset Voltage and Drift in CMOS op amps)
- ◆ **BIPOLAR (NPN) + CMOS (BiCMOS):** Bipolar Input Stage adds Linearity, Low Power, Rail-to-Rail Output
- ◆ **COMPLEMENTARY BIPOLAR + CMOS (CBiCMOS):** Rail-to-Rail Inputs, Rail-to-Rail Outputs, Good Linearity, Low Power, Higher Cost

Op Amp Applications, Chapter 1

1.39

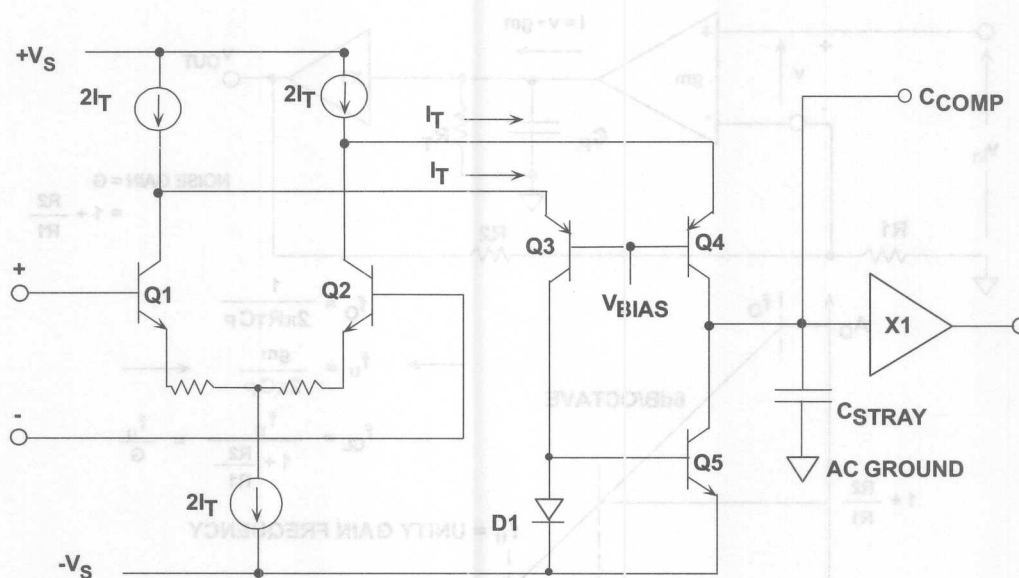
AMPLIFIER BANDWIDTH VERSUS SUPPLY CURRENT FOR ANALOG DEVICES' PROCESSES



Op Amp Applications, Chapter 1

1.40

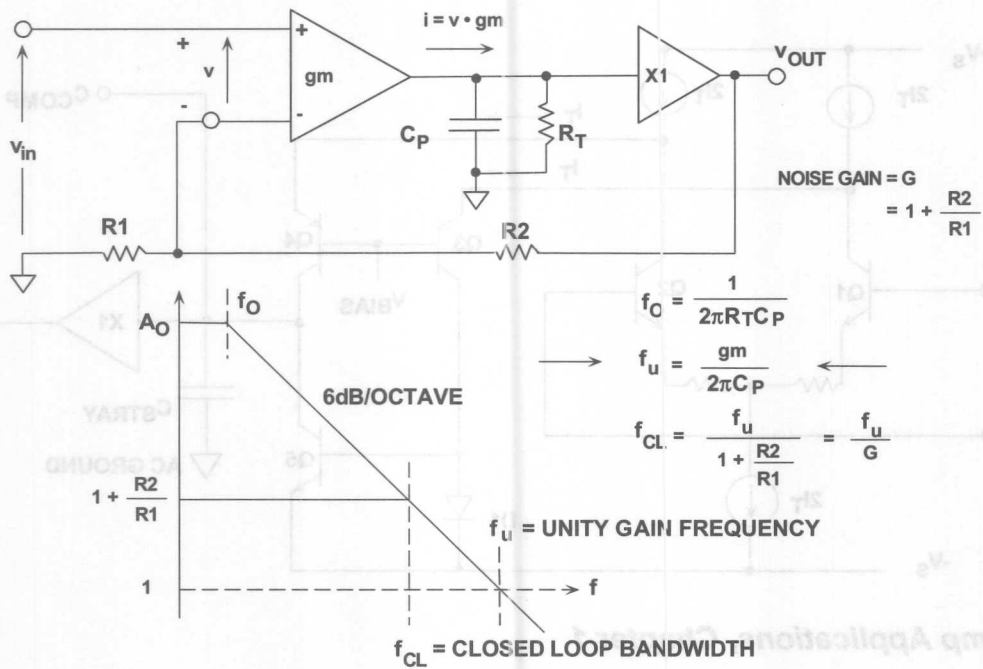
FOLDED CASCODE SIMPLIFIED CIRCUIT

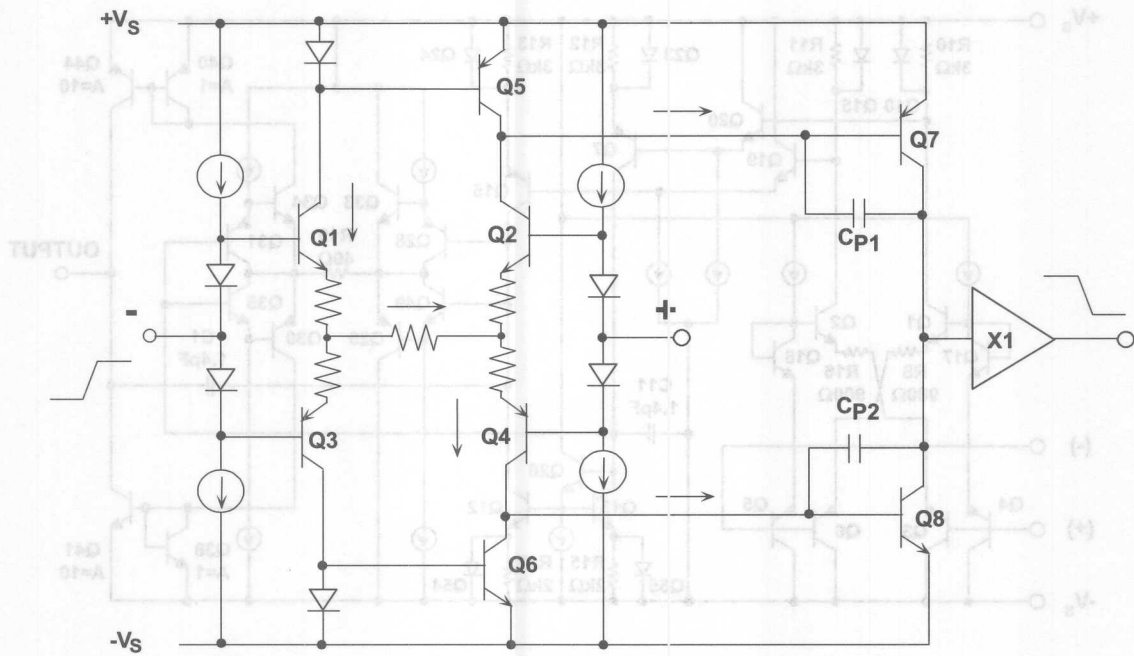


Op Amp Applications, Chapter 1

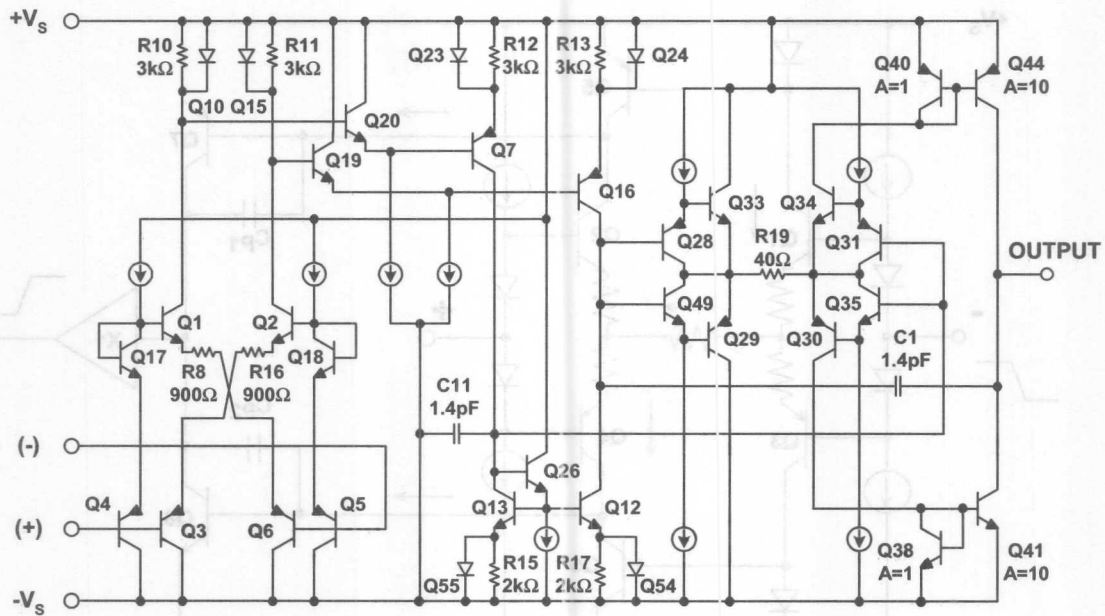
1.41

MODEL AND BODE PLOT FOR A VFB OP AMP



**"QUAD-CORE" VFB gm STAGE FOR
CURRENT-ON-DEMAND***Op Amp Applications, Chapter 1***1.43**

AD8061/62/63 SINGLE-SUPPLY 300MHz VOLTAGE FEEDBACK OP AMP

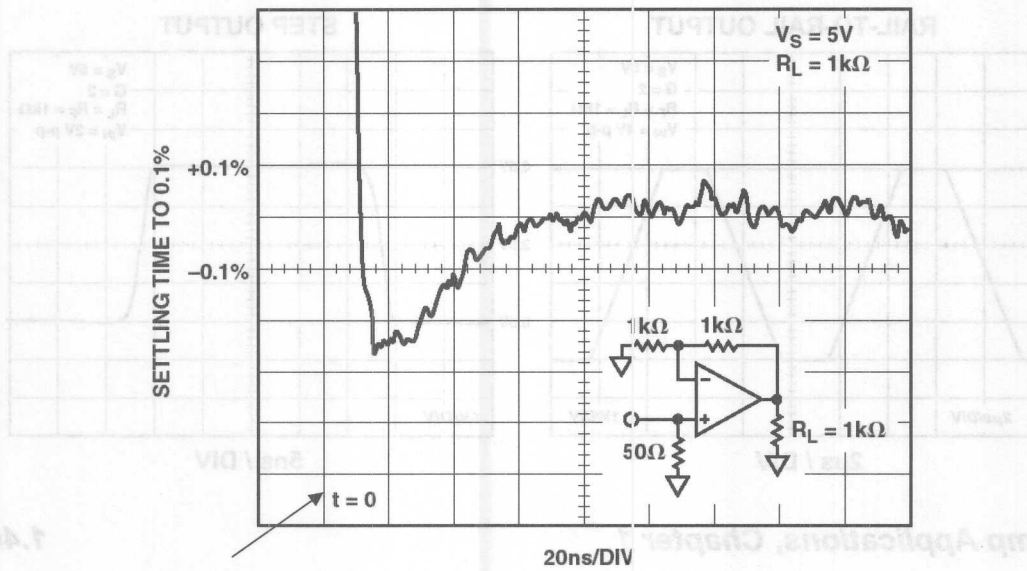


Op Amp Applications, Chapter 1

1.44

AD8061 OUTPUT SETTLING TIME

$G = +2$, $V_S = +5V$

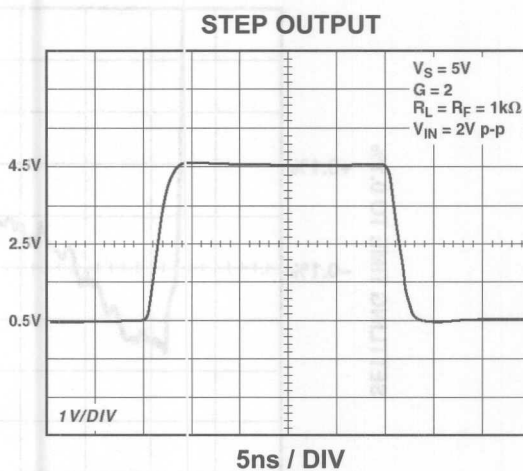
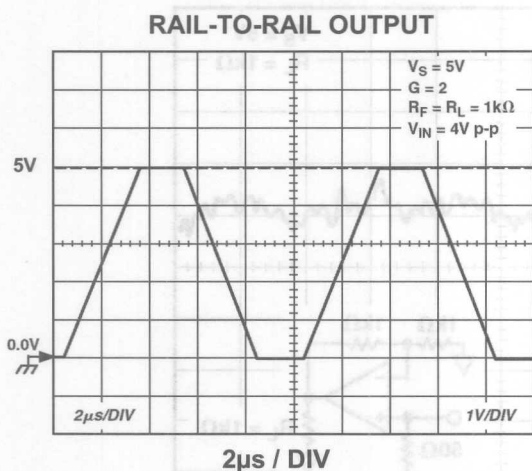


Op Amp Applications, Chapter 1

1.45

AD8061 OUTPUT RESPONSE

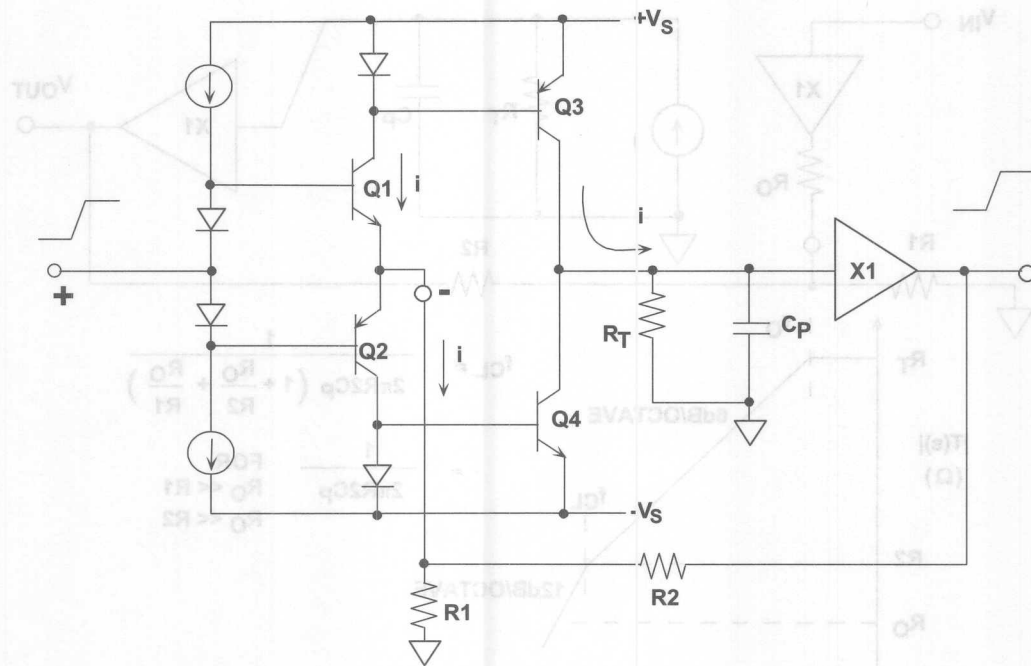
$G = +2$, $V_S = +5V$



Op Amp Applications, Chapter 1

1.46

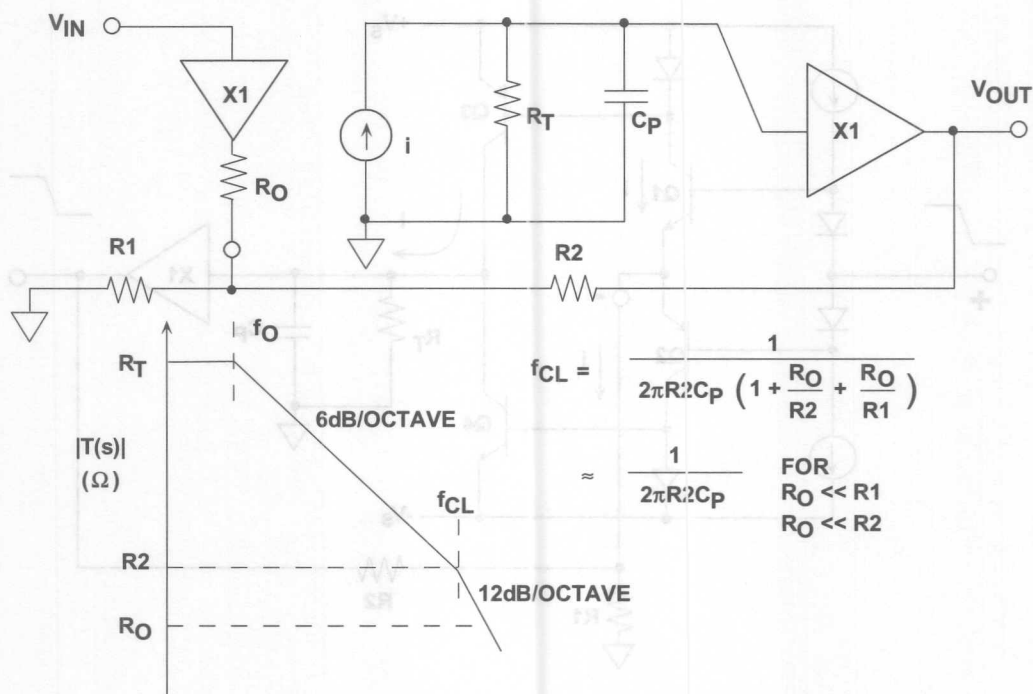
SIMPLIFIED CURRENT FEEDBACK (CFB) OP AMP



Op Amp Applications, Chapter 1

1.47

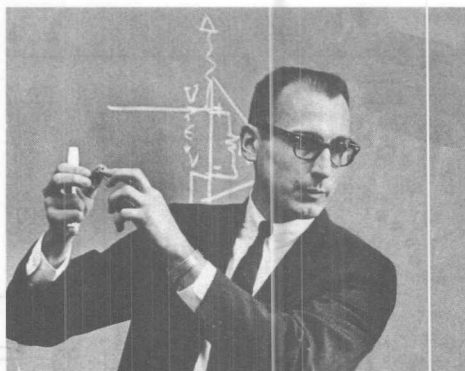
CFB OP AMP MODEL AND BODE PLOT



Op Amp Applications, Chapter 1

1.48

RAY STATA PUBLICATIONS ESTABLISH ADI APPLICATIONS WORK



1. Ray Stata, "Operational Amplifiers-Parts I and II," *Electromechanical Design*, Sept., Nov., 1965.
2. Ray Stata, "Operational Integrators," *Analog Dialogue*, Vol. 1, No. 1, April, 1967.
See also ADI AN357
3. Ray Stata, "User's Guide to Applying and Measuring Operational Amplifier Specifications," *Analog Dialogue*, Vol. 1, No. 3, September 1967. See also ADI AN356.
4. Ray Stata, "Applications Manual for 201, 202, 203 and 210 Chopper Op Amps," ADI, 1967.
5. "Ray Stata Speaks Out on 'What's Wrong with Op Amp Specs'," *EEE*, July 1968.

Op Amp Applications, Chapter 1

1.50

ADI APPLICATIONS: 2002

<http://www.analog.com>

- ◆ Analog Dialogue
- ◆ Application Notes, Article Reprints
- ◆ White Papers
- ◆ Tutorials
- ◆ Product Selection Guides
- ◆ CD ROM Catalog
- ◆ Short Form Designers' Guide
- ◆ New Products Book
- ◆ ADI Technical Library
- ◆ Seminar Books on www:
 - Practical Analog Design Techniques
 - Power and Thermal Management
 - High Speed Design Techniques
 - Sensor Signal Conditioning
 - Mixed-Signal and DSP Design Techniques
- ◆ 1-800-ANALOGD

1.51

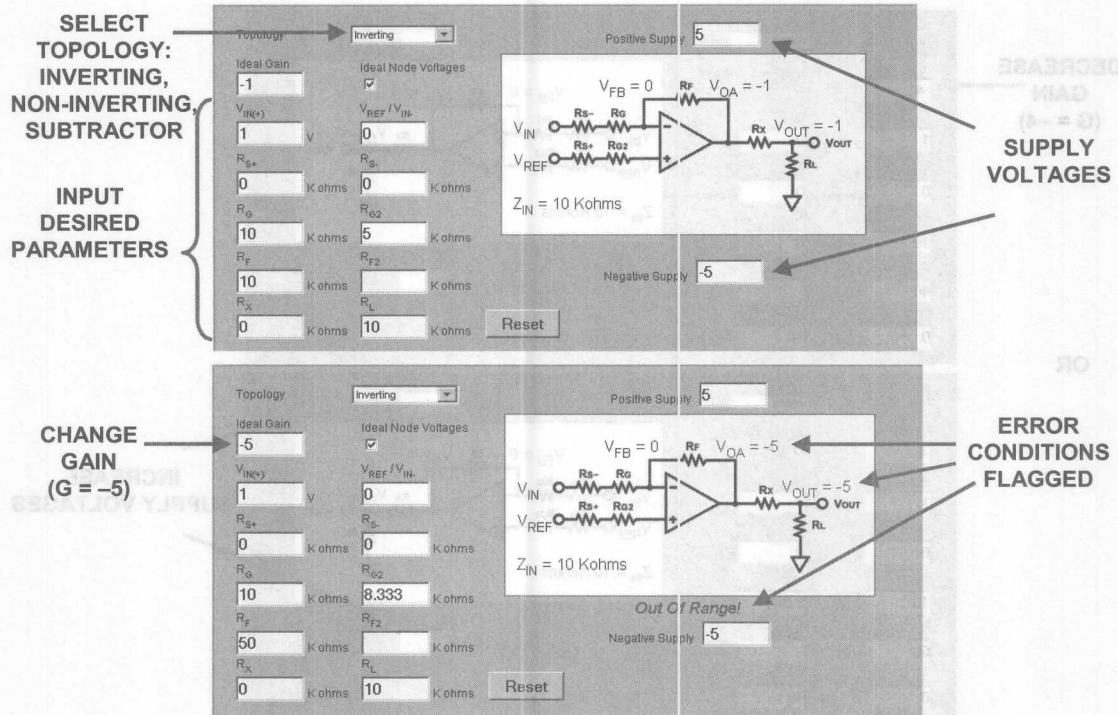
ADI WEB-BASED INTERACTIVE DESIGN TOOLS

<http://www.analog.com/techSupport/DesignTools/index.html>

- ◆ Op Amp
 - Gain/Range Error Calculator
 - Error Budget Analysis
- ◆ In-Amp
 - Gain/Range Error Calculator
 - Error Budget Analysis
- ◆ Differential Amplifiers
 - Gain/Range Error Calculator
- ◆ Ideal Single Pole Op Amp Stability Analysis
- ◆ Log Amp: Output Voltage and Impedance Matching
- ◆ ADC Tools
- ◆ DAC/DDS/PLL Tools
- ◆ Accelerometer Tools
- ◆ Transmission Line Matching Tutorial
- ◆ Filter Design

1.52

OP AMP RANGE/GAIN/ERROR CALCULATOR



OP AMP RANGE/GAIN/ERROR CALCULATOR CONTINUED

DECREASE GAIN (G = -4)

OR

INCREASE SUPPLY VOLTAGES

Topology:

Positive Supply:

Negative Supply:

Reset

Ideal Gain:

Ideal Node Voltages: ☒

$V_{IN} = 1$ V

$V_{REF} / V_{IN} = 0$

$R_{S+} = 0$ K ohms

$R_{S-} = 0$ K ohms

$R_{G1} = 10$ K ohms

$R_{G2} = 8$ K ohms

$R_F = 40$ K ohms

$R_{F2} =$ K ohms

$R_X = 0$ K ohms

$R_L = 10$ K ohms

$Z_{IN} = 10$ Kohms

$V_{FB} = 0$

$V_{OA} = -4$

$V_{OUT} = -4$

V_{REF}

V_{IN}

R_{S+}

R_{S-}

R_{G1}

R_{G2}

R_F

R_{F2}

R_X

R_L

Topology:

Positive Supply:

Negative Supply:

Reset

Ideal Gain:

Ideal Node Voltages: ☒

$V_{IN} = 1$ V

$V_{REF} / V_{IN} = 0$

$R_{S+} = 0$ K ohms

$R_{S-} = 0$ K ohms

$R_{G1} = 10$ K ohms

$R_{G2} = 8.333$ K ohms

$R_F = 50$ K ohms

$R_{F2} =$ K ohms

$R_X = 0$ K ohms

$R_L = 10$ K ohms

$Z_{IN} = 10$ Kohms

$V_{FB} = 0$

$V_{OA} = -5$

$V_{OUT} = -5$

V_{REF}

V_{IN}

R_{S+}

R_{S-}

R_{G1}

R_{G2}

R_F

R_{F2}

R_X

R_L

OP AMP ERROR BUDGET ANALYSIS FOR OP1177

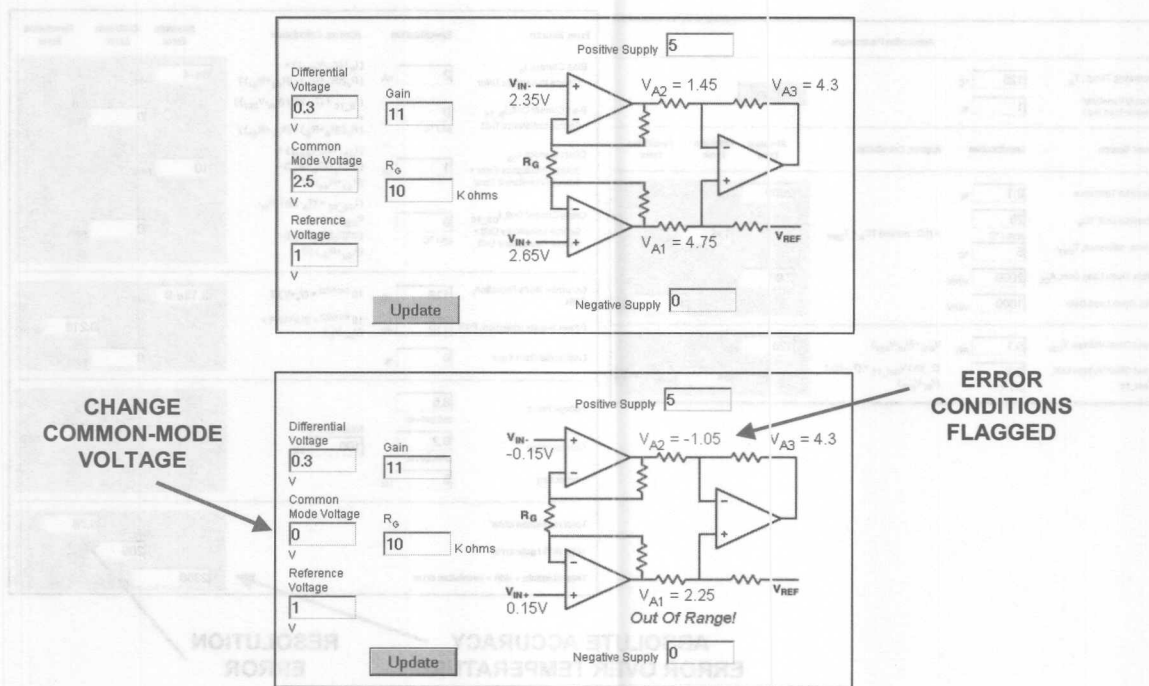
Application Parameters					
Operating Temp., T_A	125 °C	Update			
Supply Variability (ripple-load reg.)	1 %				
Error Source	Specification	Approx. Calculation	Absolute Error	Drift/Gain Error	Resolution Error
Resistor Tolerance	0.1 %		2000 ppm		
Resistor Drift, TC_R	25 ppm/°C	$-(1/2 \cdot \text{noninj}) TC_R \times T_{\text{diff}}$		125 ppm	
Temp. difference, T_{diff}	5 °C				
Nom. Open Loop Gain, A_{OL}	2000 V/mV		2.99 ppm		
Min. Open Loop Gain	1000 V/mV				3 ppm
Input Offset Voltage, V_{OSI}	0.1 mV	$V_{OSI} / (V_{IN} V_{REF})$	120 ppm		
Input Offset Voltage Drift, V_{OSI_TC}	0.7 $\mu\text{V}/^\circ\text{C}$	$(2 \cdot \text{inv}) V_{OSI_TC} \times (T_A - 25) / (V_{IN} V_{REF})$		84 ppm	
Error Source	Specification	Approx. Calculation	Absolute Error	Drift/Gain Error	Resolution Error
Bias Current, I_B	2 nA	$(I_B / (V_{IN} V_{REF})) \times (R_F R_O + R_S) - (R_{O2} + R_{S2})$	8e-4 ppm		
- Source Imbalance Error					
Bias Current Drift, I_{B_TC}	0 pA/°C	$(I_{B_TC} \times (T_A - 25) / (V_{IN} V_{REF})) \times (R_F R_O + R_S) - (R_{O2} + R_{S2})$		0 ppm	
- Source Imbalance Error					
Offset Current, I_{OS}	1 nA	$(I_{OS} / (V_{IN} V_{REF})) \times (R_F R_O + R_S) - (R_{O2} + R_{S2})$	10 ppm		
- Source Imbalance Error + Source Resistance Error					
Offset Current Drift, I_{OS_TC}	0 pA/°C	$(I_{OS_TC} \times (T_A - 25) / (V_{IN} V_{REF})) \times (R_F R_O + R_S) - (R_{O2} + R_{S2})$		0 ppm	
- Source Imbalance Error + Source Resistance Error					
Common Mode Rejection, CMR	118 dB	$10 \text{ CMR}/20 \times (V_A + V)/2$	3.15e-9 ppm		
Power Supply Rejection, PSR	115 dB	$10 \text{ PSR}/20 \times \text{SUP-VAR} \times (V_{S+} - V_{S-})$		0.213 ppm	
Differential Gain Error	0 %			0 ppm	
Voltage noise	8.5 nV/root-Hz	Noise BW: 0.1 - 100 Hz			3.57 ppm
Current noise	0.2 pA/root-Hz				
Corner freq	5 Hz				
Total resolution error					6.78 ppm
Total drift / gain error				209 ppm	
Total absolute + drift + resolution error			2350 ppm		

**ABSOLUTE ACCURACY
ERROR OVER TEMPERATURE**

**RESOLUTION
ERROR**

1.55

AD623 SINGLE SUPPLY IN AMP RANGE/GAIN/ERROR CALCULATOR EXAMPLE



AD623 ERROR BUDGET

Application Parameters			
Differential Amplitude, V_{DIFF}	10 mV	Common Mode Voltage, V_{COMM}	2.5 V
Gain	100	Operating Temperature, T_A	85 °C
Source Impedance R_{S+}	100 ohms	R_{S-}	0 ohms
<input type="button" value="Calculate"/>			

Error Source	Specification	Calculation	Effect on Absolute Accuracy	Effect on Resolution at Temp.
Gain Error	0.35 %		3500 ppm	
Gain Drift, G_{TC}	50 ppm/°C	$G_{TC} * (T_A - 25)$	3000 ppm	
Gain Nonlinearity	0.0050 %		50 ppm	
Input Offset Voltage, V_{OSI}	160 μ V	V_{OSI} / V_{DIFF}	16000 ppm	
Input Offset Voltage Drift, V_{OSI_TC}	1.0 μ V/°C	$(V_{OSI_TC} / V_{DIFF}) * (T_A - 25)$	6000 ppm	
Output Offset Voltage, V_{OSO}	1.1 mV	$V_{OSO} / (GAIN * V_{DIFF})$	1100 ppm	
Output Offset Voltage Drift, V_{OSO_TC}	10 μ V/°C	$(V_{OSO_TC} / (GAIN * V_{DIFF})) * (T_A - 25)$	600 ppm	

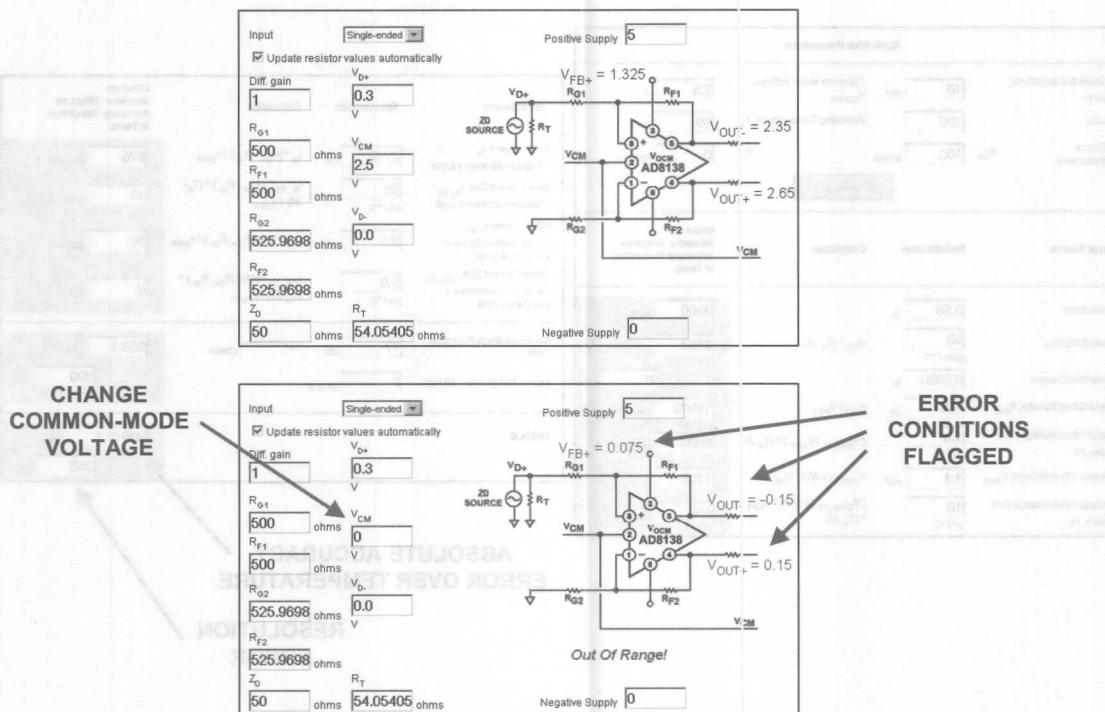
Error Source	Specification	Calculation	Effect on Absolute Accuracy	Effect on Resolution at Temp.
Bias Current I_B - Source Imbalance Error	27.5 nA	$I_B * (R_{S+} + R_{S-}) / V_{DIFF}$	275 ppm	
Bias Current Drift, I_{B_TC} - Source Imbalance Drift	25 pA/°C	$I_{B_TC} * (R_{S+} + R_{S-}) * (T_A - 25) / V_{DIFF}$	15 ppm	
Offset Current, I_{OS} - Source Resistance Imbalance Error	2.5 nA	$I_{OS} * MAX(R_{S+}, R_{S-}) / V_{DIFF}$	30 ppm	
Offset Current Drift, I_{OS_TC} - Source Resistance Imbalance Drift	5.0 pA/°C	$I_{OS_TC} * MAX(R_{S+}, R_{S-}) * (T_A - 25) / V_{DIFF}$	0 ppm	
Common Mode Rejection, CMR	77 dB	$10^{CMR/20} * V_{COMM}$	353.1 ppm	
Noise, RTI (0.1 Hz - 10 Hz)	3 μ V p-p		300 ppm	
TOTALS			30873.1 ppm	350 ppm

ABSOLUTE ACCURACY
ERROR OVER TEMPERATURE

RESOLUTION
ERROR

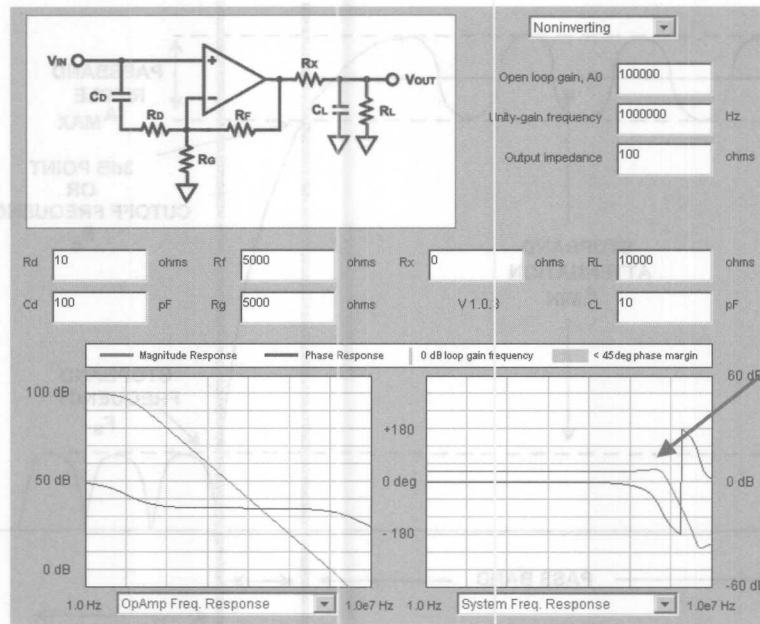
1.57

AD8138 DIFFERENTIAL AMPLIFIER RANGE/GAIN/ERROR CALCULATOR



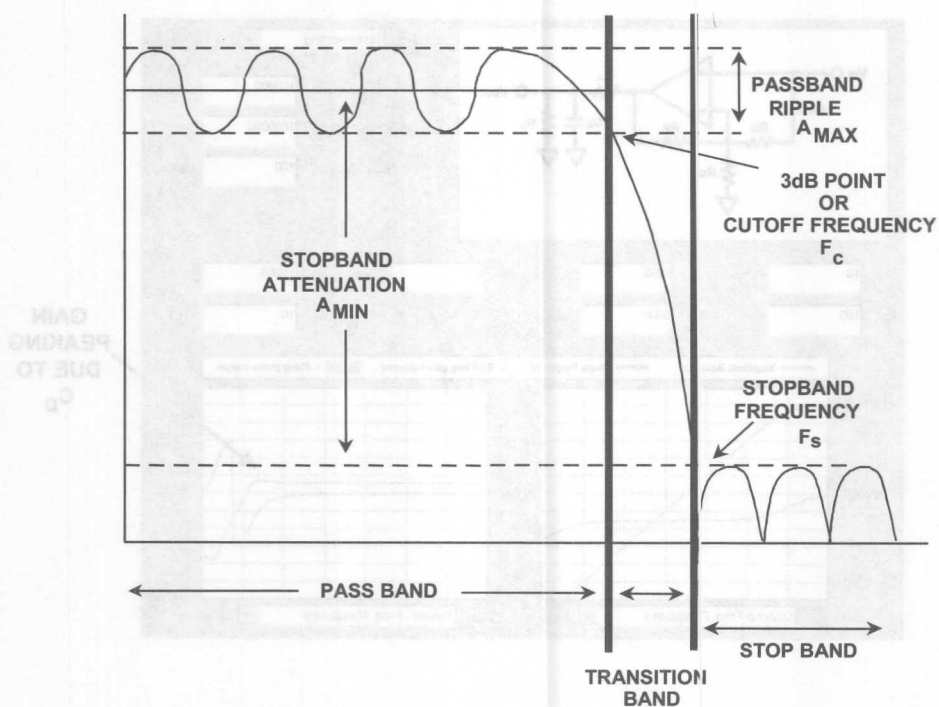
1.58

SINGLE-POLE OP AMP MODEL GAIN AND PHASE RESPONSE



1.59

KEY FILTER PARAMETERS



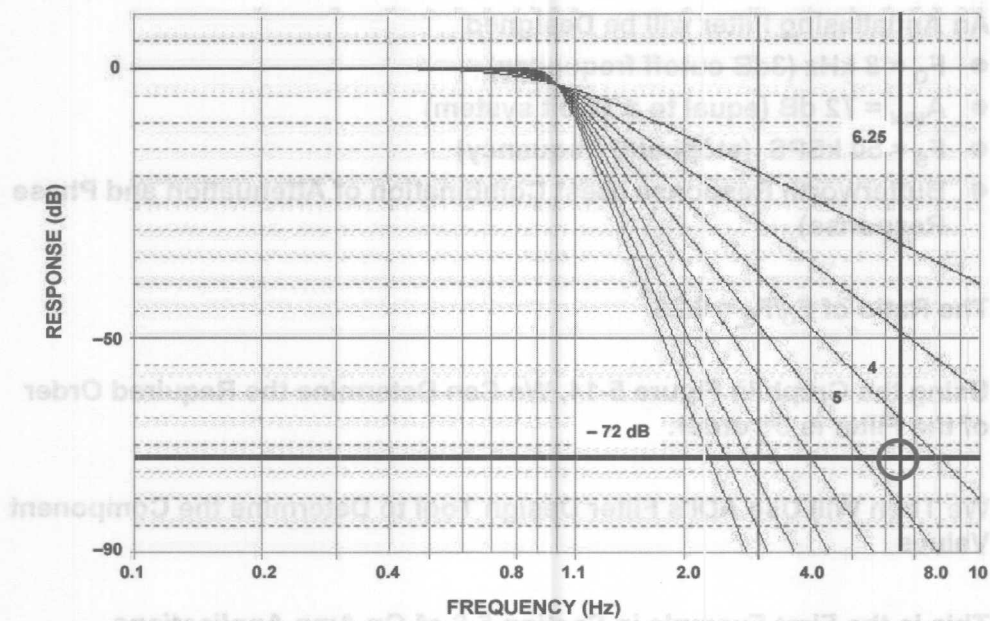
ANTIALIASING FILTER DESIGN EXAMPLE

- ◆ An Antialiasing Filter will be Designed
 - $F_O = 8 \text{ kHz}$ (3dB cutoff frequency)
 - $A_{\text{MIN}} = 72 \text{ dB}$ (equal to a 12 bit system)
 - $F_S = 50 \text{ kSPS}$ (stopband frequency)
 - Butterworth Response (Best Combination of Attenuation and Phase Response)
- ◆ The Ratio of $F_O/F_S = 6.25$
- ◆ Using the Graph in Figure 5-14, We Can Determine the Required Order of the Filter is 5th order.
- ◆ We Then Will Use ADI's Filter Design Tool to Determine the Component Values
- ◆ This is the First Example in Section 5-8 of *Op Amp Applications*

Op Amp Applications, Chapter 5

1.61


DETERMINING FILTER ORDER



Op Amp Applications, Chapter 5

1.62

1st SECTION FILTER DESIGN TOOL



[Home](#) | [Buy](#) | [Order Samples](#) | [Technical Support](#) | [myAnalog](#)

[ADI Home](#) > [Technical Support](#) > [Interactive Design Tools](#) >

Interactive Design Tools

Interactive Design Tools
OpAmps : Active Filter Synthesis
PROTOTYPE

[Instructions](#) | [Troubleshooting](#) | [Related Information](#) | [Send this Link to a Colleague](#)

Filter Type: Order:

f_c Hz

Stage 1:
F0 Hz
Q

Stage 2:
F0 Hz
Q

Stage 3:
F0 Hz

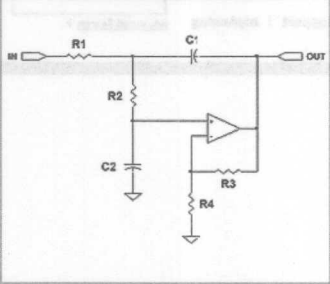
Op Amp Applications, Chapter 5

1.63

1ST SECTION DESIGN (SALLEEN-KEY)

Circuit
Mag-Phase

V0.9.4



Gain:

C1: nF

R3: ohms

R1: ohms

R3: ohms

R2: ohms

R4: ohms

C1: nF

C2: nF

Tolerance R: C:

Actual F0: 8000
Actual Q: 0.618

Actual F0: 8000
Actual Q: 1.618

Actual F0: 8002

Op Amp Applications, Chapter 5

1.64

2ND SECTION DESIGN (SALLEN-KEY)

Circuit Mag-Phase V0.9.4

Gain: 1

C1: 10 nF

R3: 0 ohms

R1: 6.438 K ohms R2: 6.438 K ohms C1: 10.0 nF C2: 0.9550 nF

R3: 0 K ohms R4: Infinity ohms

Tolerance R: Exact C: Exact

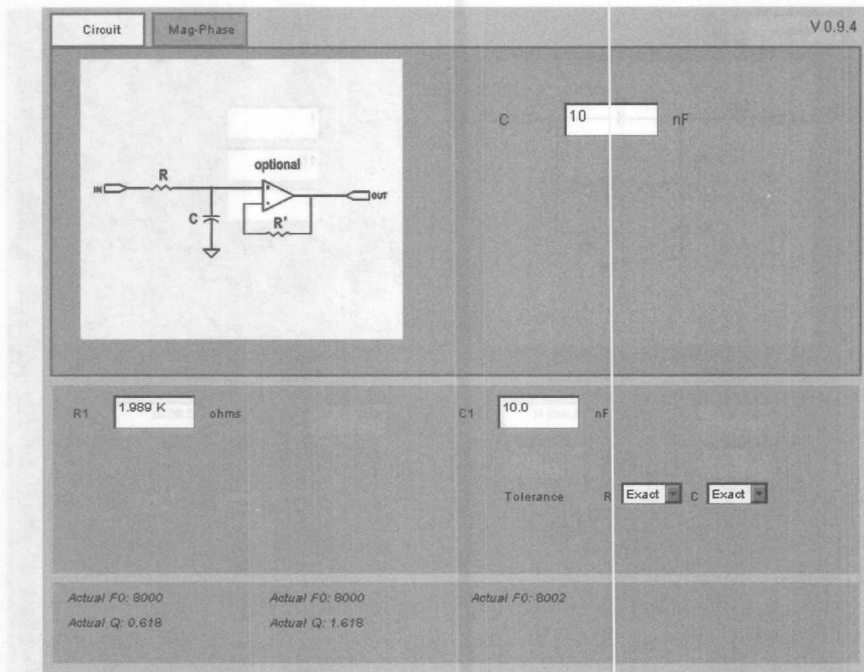
Actual F0: 8000 Actual F0: 8000 Actual F0: 8000

Actual Q: 0.618 Actual Q: 1.618

Op Amp Applications, Chapter 5

1.65

3RD SECTION DESIGN (SALLEEN-KEY)

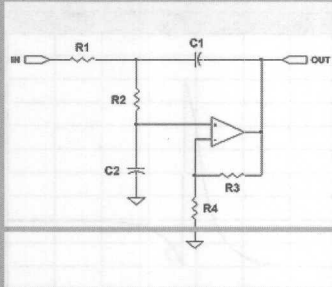


Op Amp Applications, Chapter 5

Op Amp Applications, Chapter 5 1.66

1ST SECTION WITH CLOSEST STANDARD VALUES

Circuit Mag-Phase V 0.9.4



Gain: 1

C1: 10 nF

R3: 0 ohms

R1: 2.43 K ohms R2: 2.43 K ohms C1: 10.0 nF C2: 6.2 nF

R3: 0 K ohms R4: Infinity ohms

Tolerance R: 1.0% C: 5%

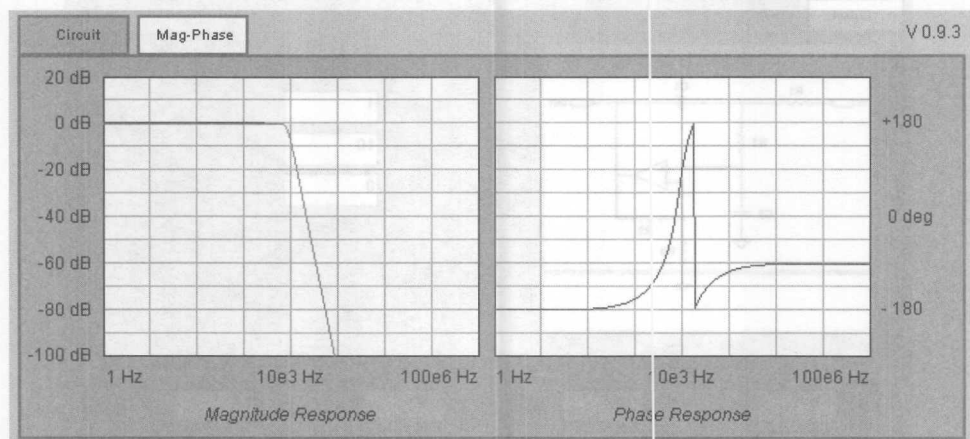
Actual F0: 8130 (1.6%) Actual F0: 7944 (-0.70%)

Actual Q: 0.6207 (0.43%) Actual Q: 1.62 (0.19%)

Op Amp Applications, Chapter 5

1.67

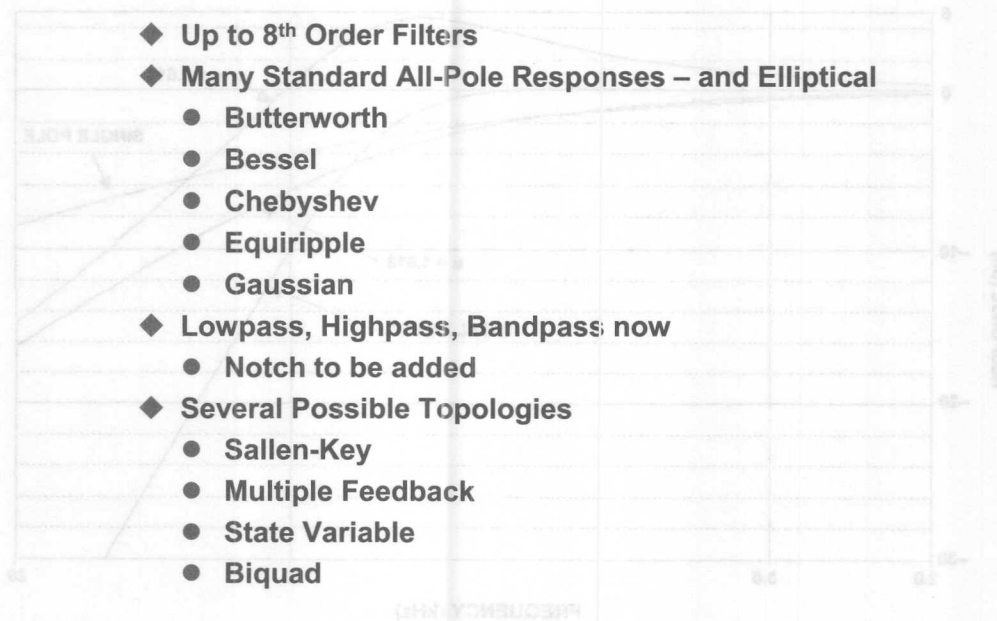
MAGNITUDE AND PHASE PLOTS



Op Amp Applications, Chapter 5

1.68

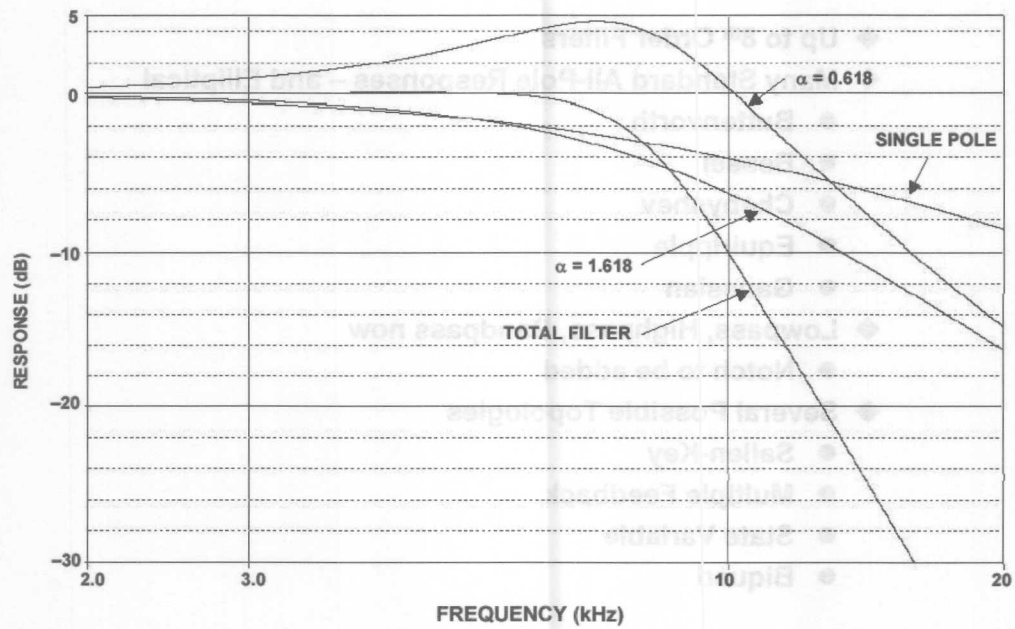
FILTER DESIGN TOOL CAPABILITIES



Op Amp Applications, Chapter 5

1.69

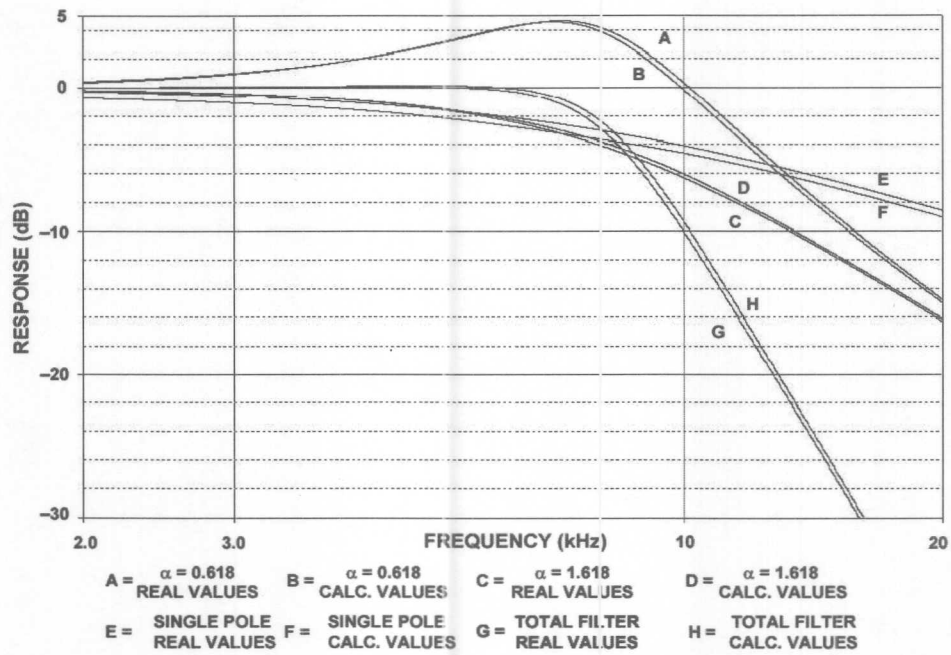
INDIVIDUAL SECTION RESPONSE



Op Amp Applications, Chapter 5

1.70

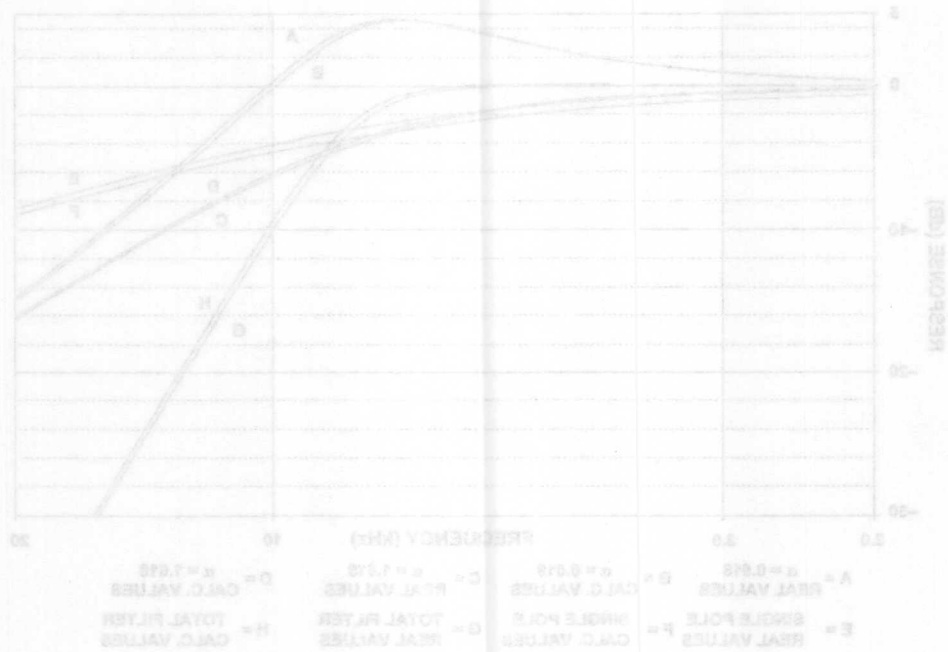
EFFECTS OF STANDARD VERSUS EXACT VALUES



Op Amp Applications, Chapter 5

1.71

EFFECTS OF STANDARD VERSUS EXACT VALUES



Op Amp Applications, Chapter 5

1.71

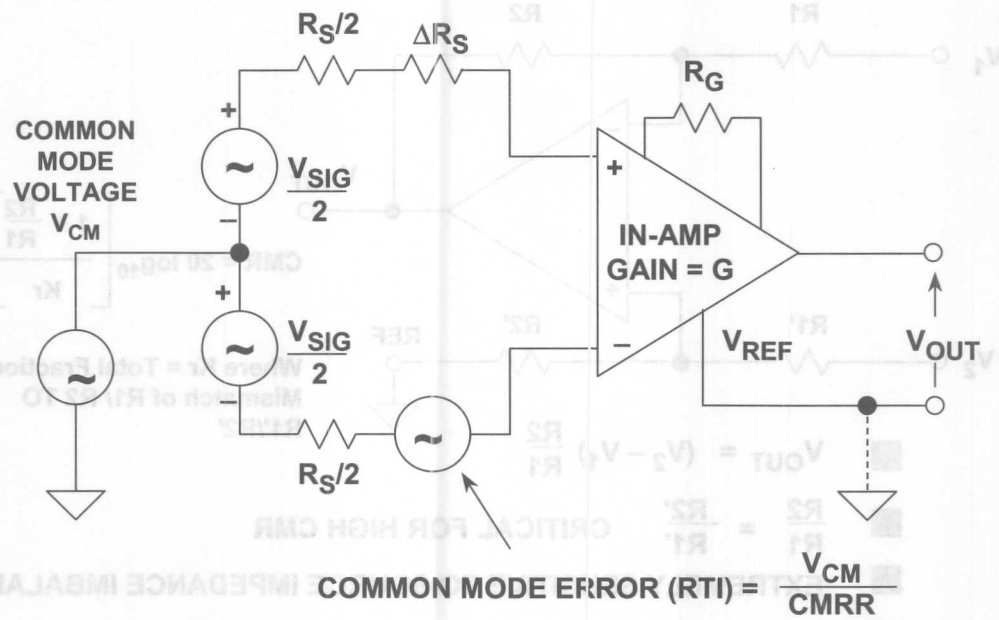
OP AMP APPLICATIONS SEMINAR

1. History, Basics, Design Aids, Filters
2. **Specialty Amplifiers, Using Op Amps with Data Converters**
3. Hardware and Housekeeping Design Techniques
4. Signal Amplifiers, Sensor Signal Conditioning

OP AMP APPLICATIONS SEMINAR

1. History, Basics, Design Aids, Filters
2. Specialty Amplifiers, Using Op Amps with Data Converters
3. Hardware and Housekeeping Design Techniques
4. Signal Amplifiers, Sensor Signal Conditioning

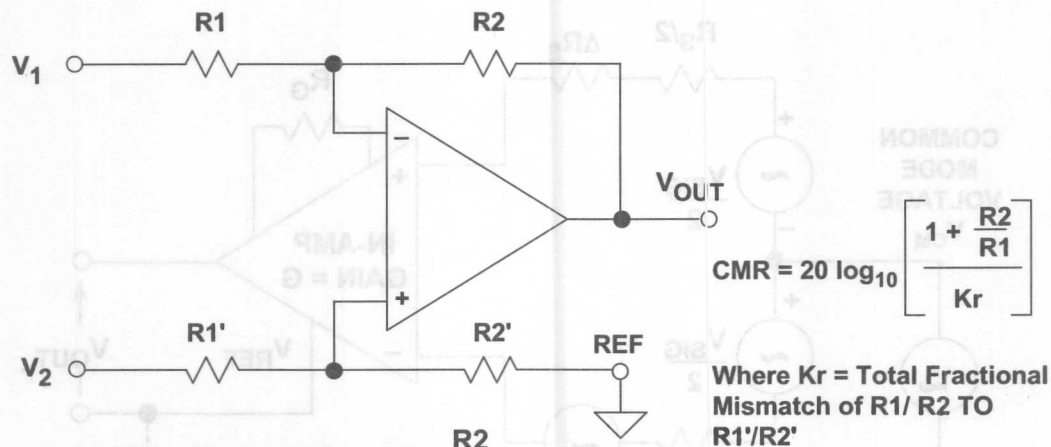
THE GENERIC INSTRUMENTATION AMPLIFIER (IN-AMP)



Op Amp Applications, Chapter 2

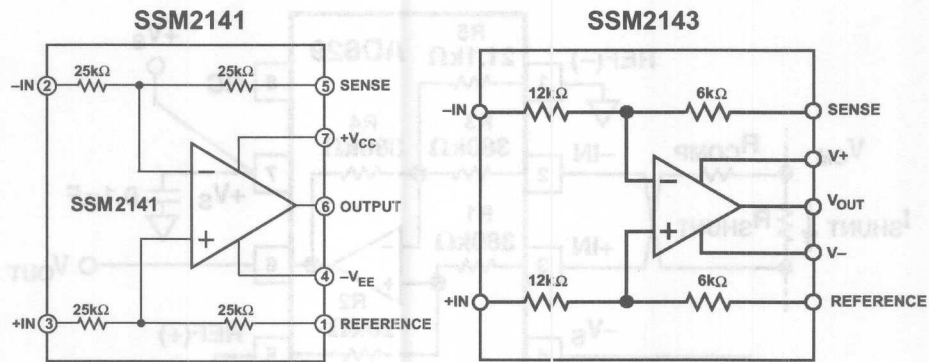
2.1

OP AMP SUBTRACTOR OR DIFFERENCE AMPLIFIER



- $V_{OUT} = (V_2 - V_1) \frac{R_2}{R_1}$
- $\frac{R_2}{R_1} = \frac{R_2'}{R_1'}$ CRITICAL FOR HIGH CMR
- EXTREMELY SENSITIVE TO SOURCE IMPEDANCE IMBALANCE
- 0.1% TOTAL MISMATCH YIELDS $\approx 66\text{dB}$ CMR FOR $R_1 = R_2$

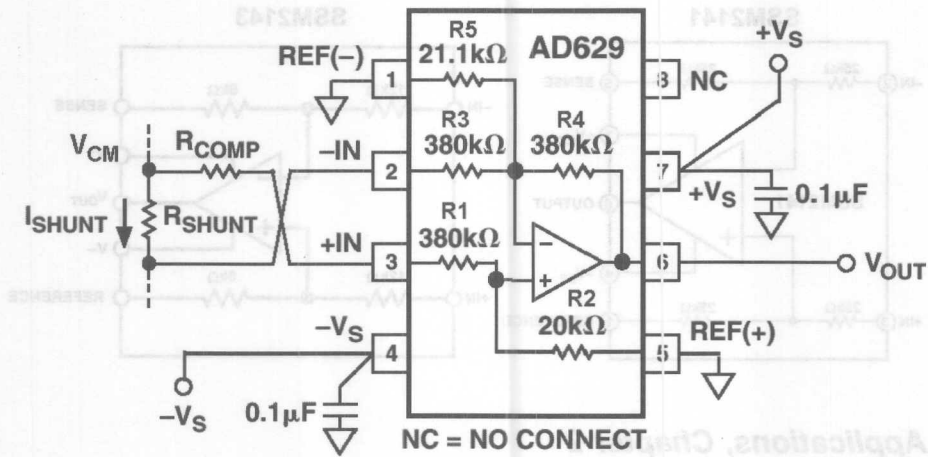
SSM2141/SSM2143 DIFFERENCE AMPLIFIERS (AUDIO LINE RECEIVERS)



Op Amp Applications, Chapter 2

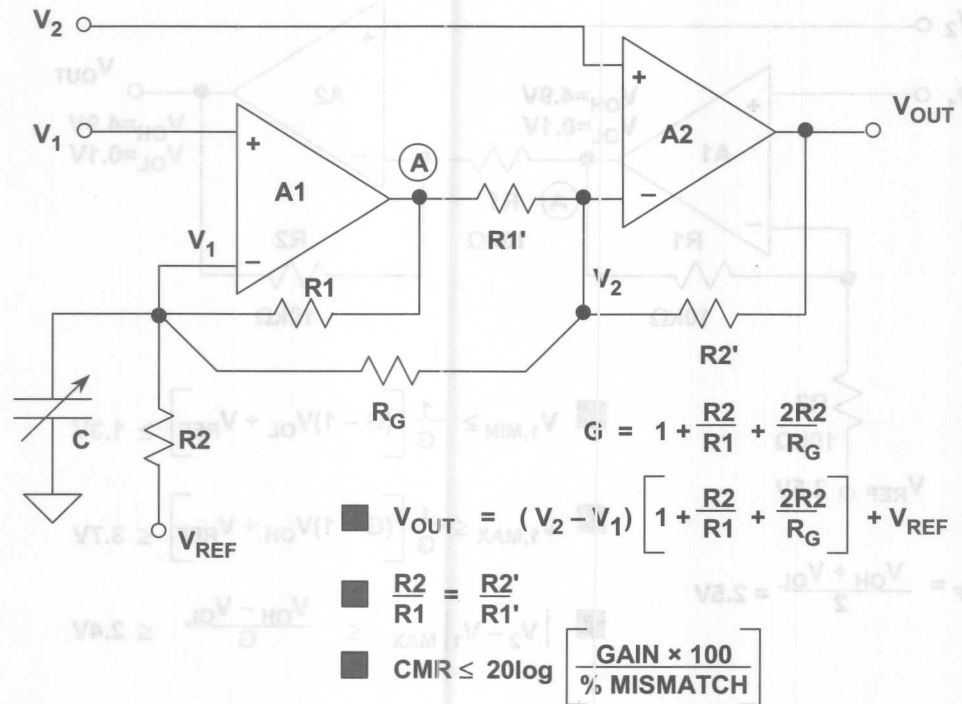
2.3

A CURRENT SENSING CIRCUIT USING THE AD629, A HIGH COMMON-MODE INPUT VOLTAGE DIFFERENCE AMPLIFIER



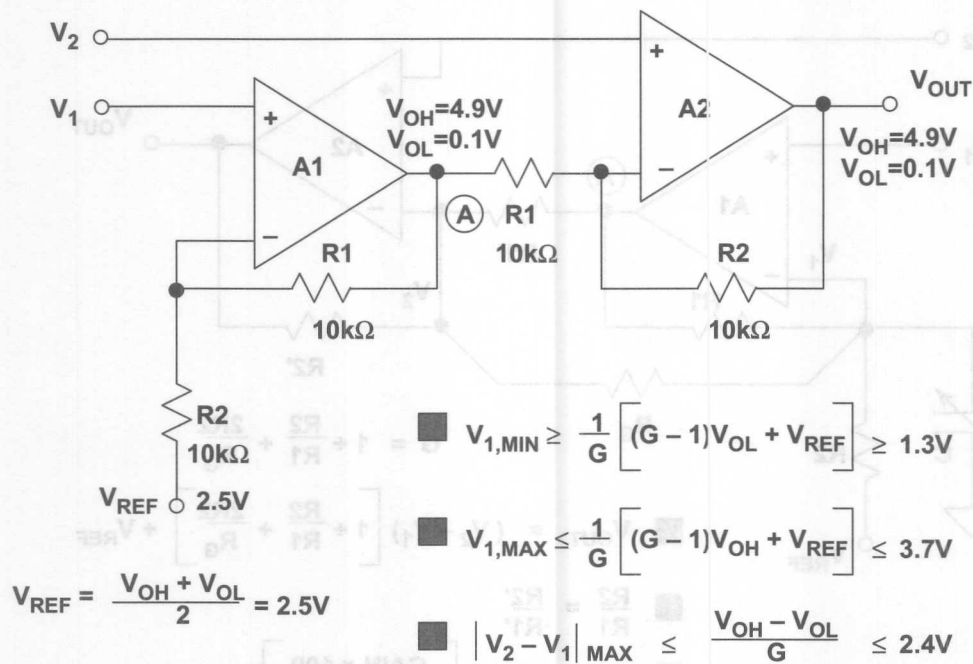
$$V_{CM} = \pm 270V \text{ for } V_S = \pm 15V$$

TWO OP AMP INSTRUMENTATION AMPLIFIER



SINGLE SUPPLY RESTRICTIONS:

$$V_S = +5V, G = 2$$

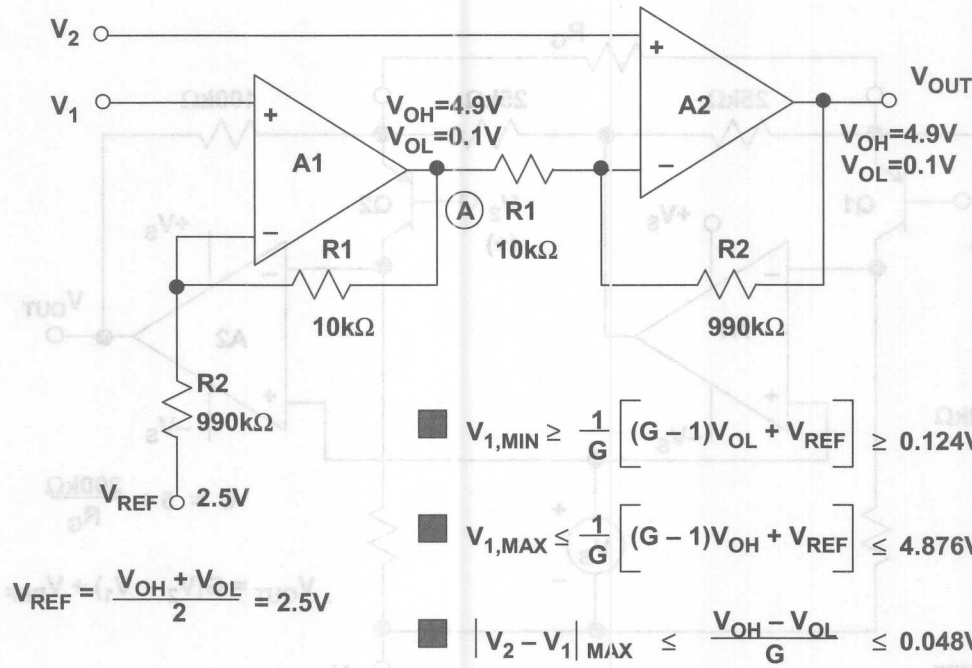


Op Amp Applications, Chapter 2

2.6

SINGLE SUPPLY RESTRICTIONS:

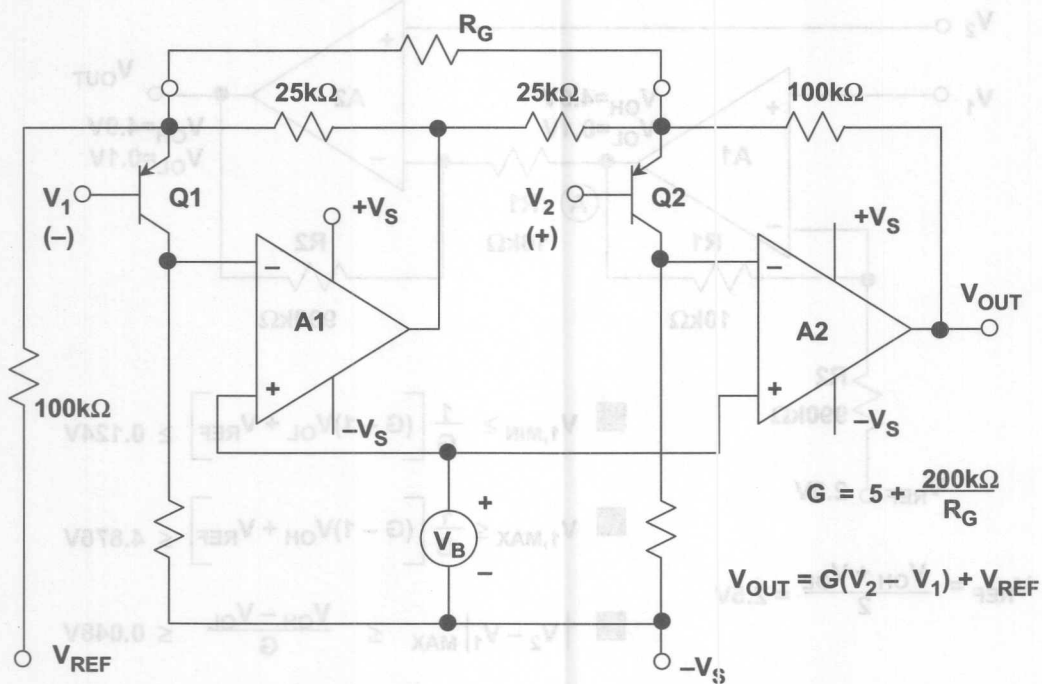
$$V_S = +5V, G = 100$$



Op Amp Applications, Chapter 2

2.7

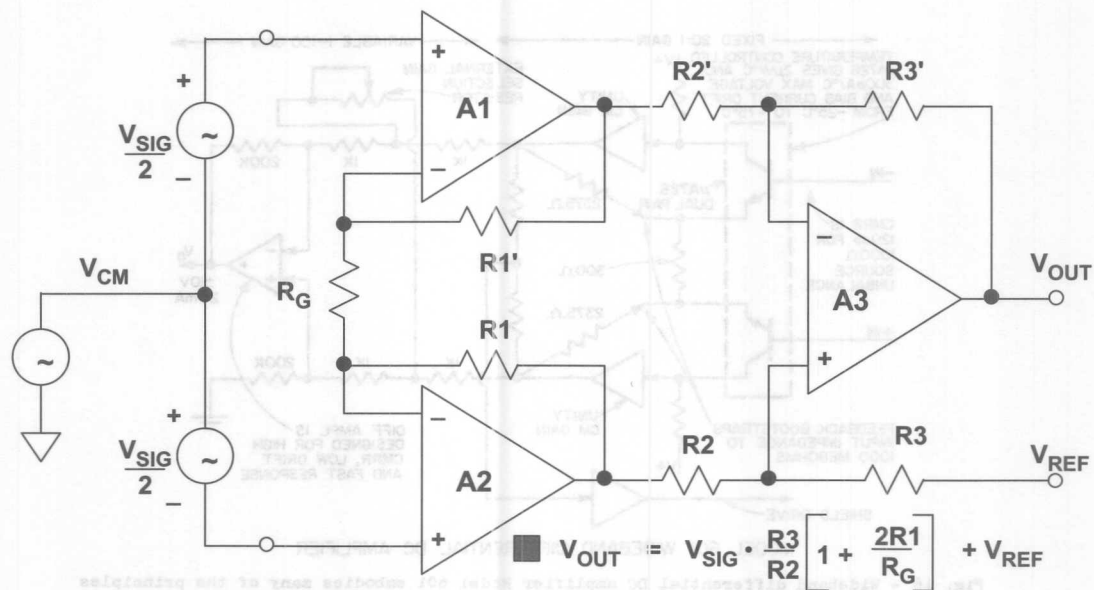
THE AD627 SINGLE-SUPPLY IN-AMP ARCHITECTURE



Op Amp Applications, Chapter 2

2.8

THREE OP AMP INSTRUMENTATION AMPLIFIER



$$CMR \leq 20 \log \left[\frac{GAIN \times 100}{\% \text{ MISMATCH}} \right]$$

$$\text{IF } R_2 = R_3, G = 1 + \frac{2R_1}{R_G}$$

Op Amp Applications, Chapter 2

2.9

ROBERT DEMROW'S 1968 "EVOLUTION FROM OPERATIONAL AMPLIFIER TO DATA AMPLIFIER"

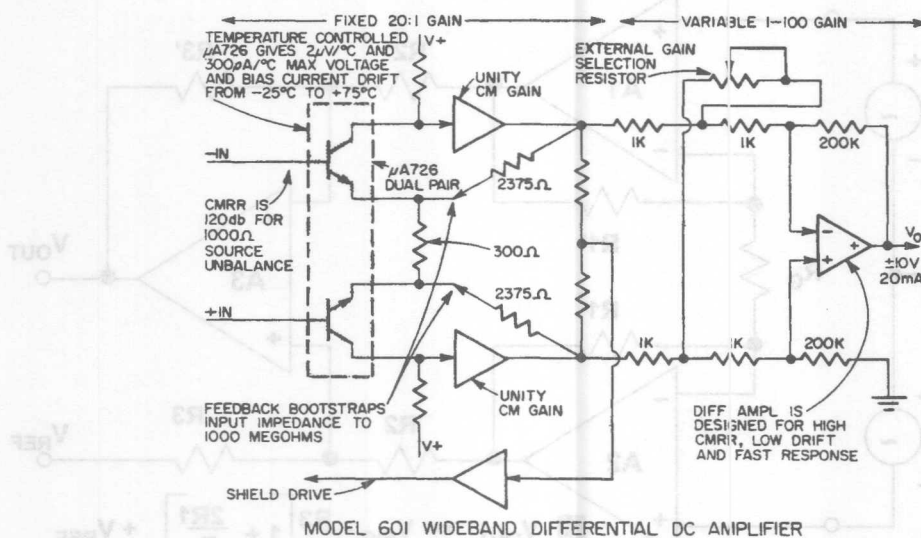
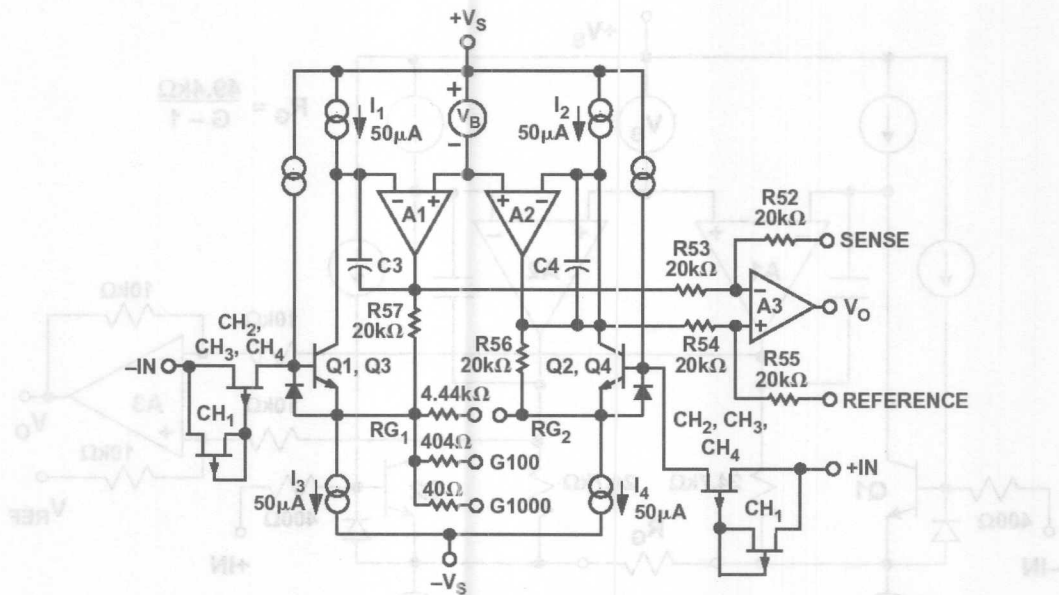


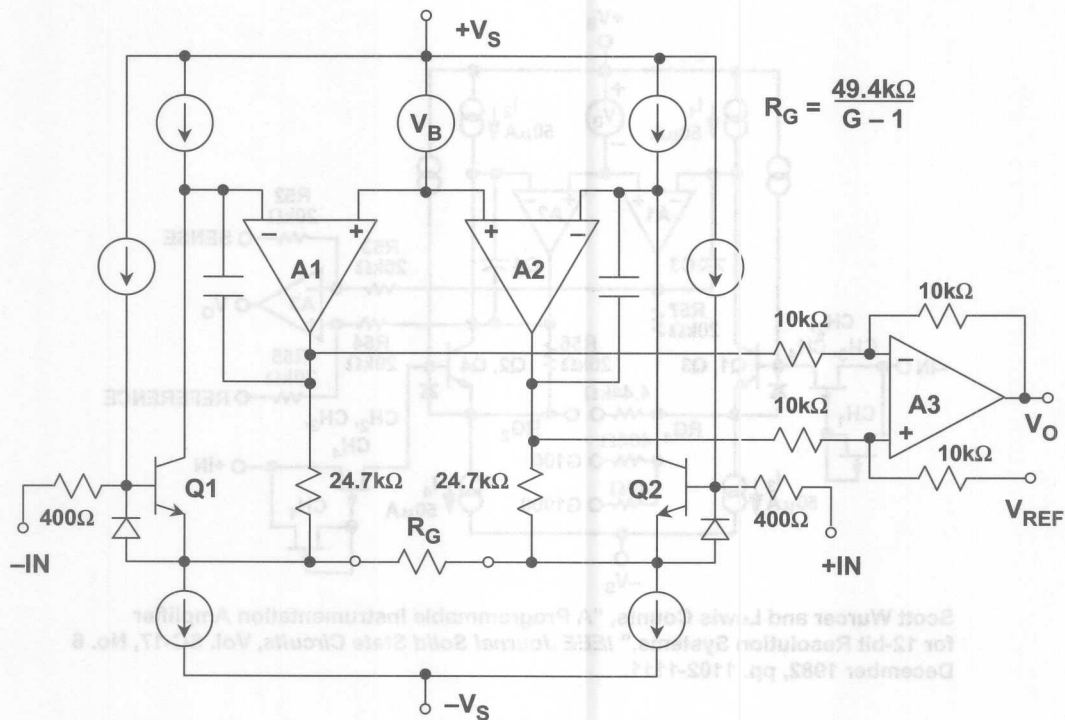
Fig. 16 - Wideband differential DC amplifier Model 601 embodies many of the principles outlined in this article. Input circuit based on $\mu A726$ temperature compensated monolithic pair provides high voltage & current stability, uses bootstrapping feedback to create 1000 megohms common mode and 10 megohms differential input impedance. Subsequent circuitry preserves $\mu A726$'s inherently-wide bandwidth by using low-value resistors, which also permit highest resistance stability, hence best long-term CMRR. Single resistor adjusts closed-loop gain from 20 to 2000; fixed first-stage gain of 20:1 reduces second stage's gain-inequality error: $CMRR_A = A/(A_2 - A_1)$, twentyfold.

AD524 RELEASED IN 1982 SET THE STANDARD FOR IC IN-AMPS



Scott Wurcer and Lewis Counts, "A Programmable Instrumentation Amplifier for 12-bit Resolution Systems," *IEEE Journal Solid State Circuits*, Vol. SC-17, No. 6 December 1982, pp. 1102-1111.

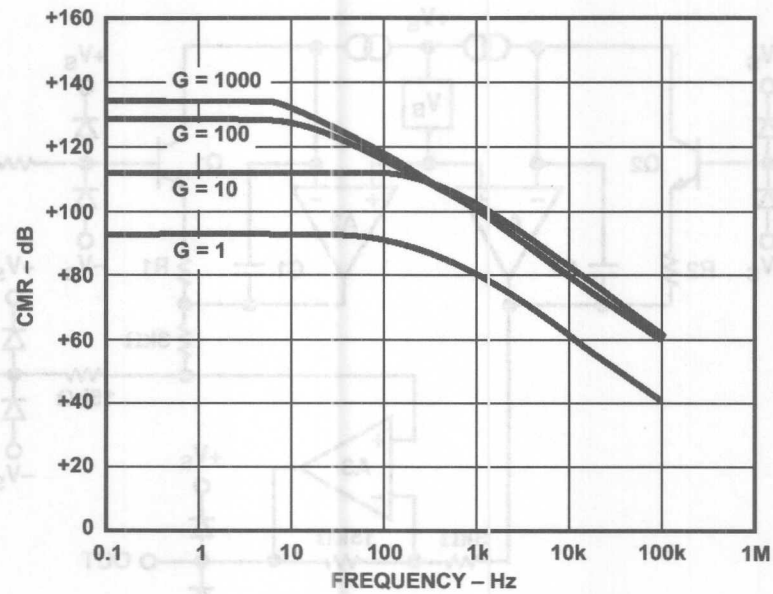
AD620 IN-AMP SIMPLIFIED SCHEMATIC (RELEASED IN 1992)



Op Amp Applications, Chapter 2

2.12

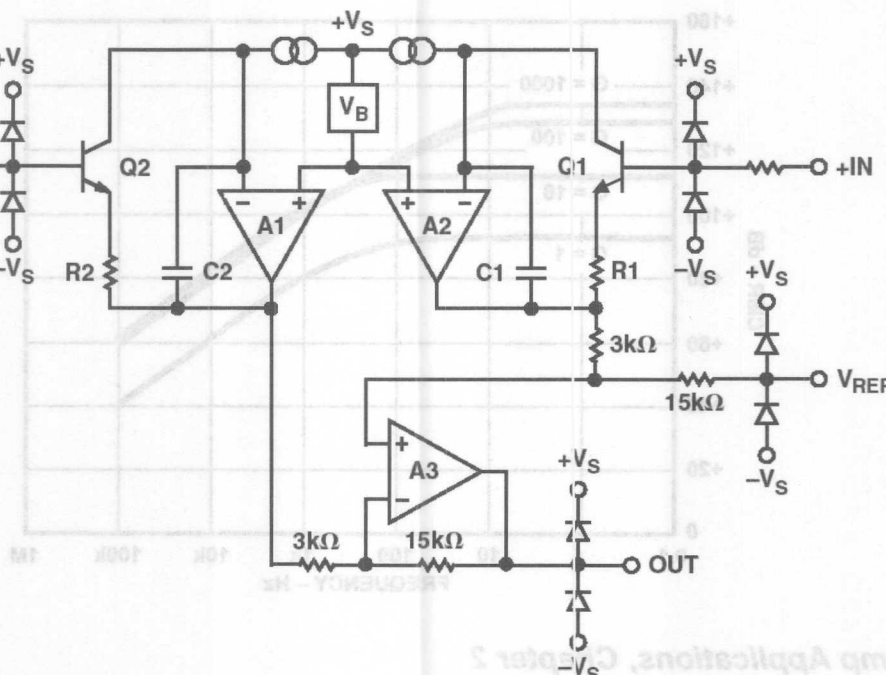
AD620 IN-AMP CMR VERSUS FREQUENCY (1k Ω SOURCE IMBALANCE)



Op Amp Applications, Chapter 2

2.13

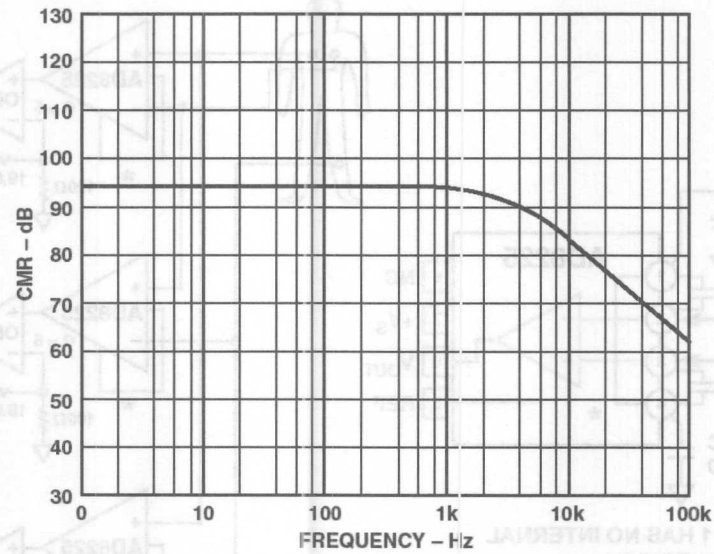
PRECISION G = 5 IN-AMP SIMPLIFIED SCH



Op Amp Applications, Chapter 2

2.14

AD8225 IN-AMP COMMON-MODE REJECTION

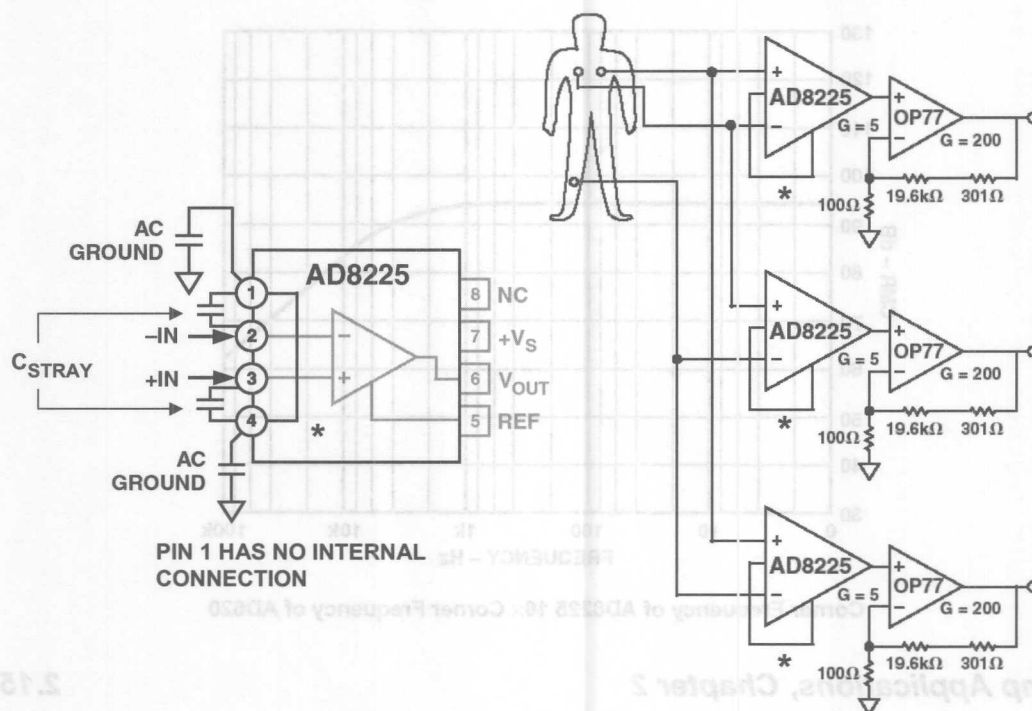


Corner Frequency of AD8225 10× Corner Frequency of AD620

Op Amp Applications, Chapter 2

2.15

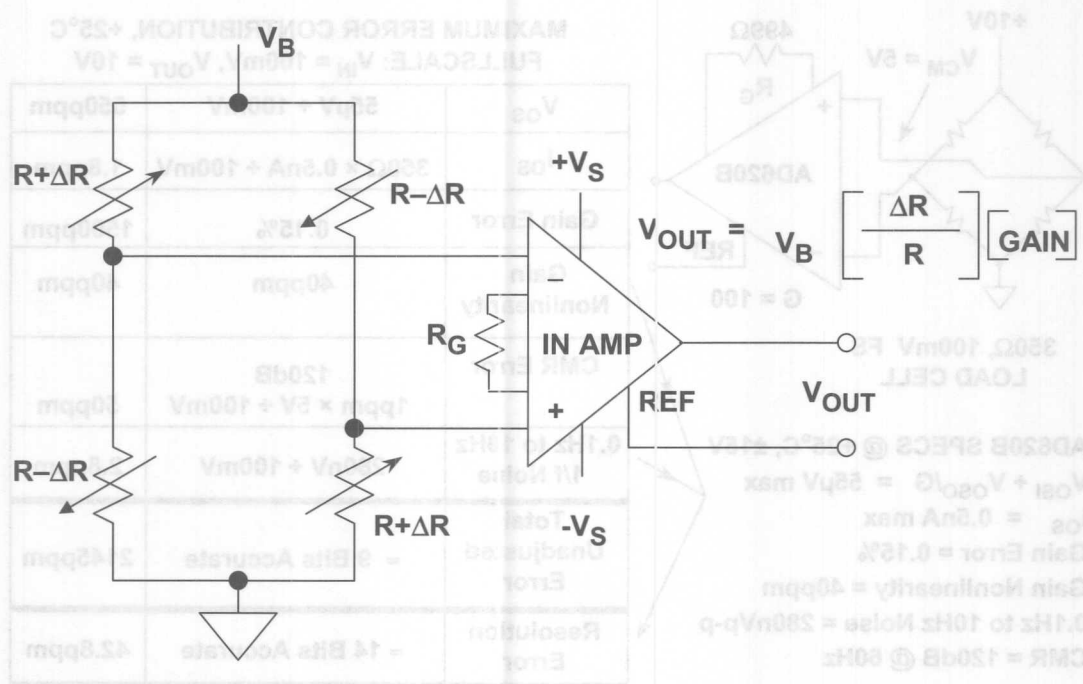
EKG MONITOR FRONT END USING THE AD8225 IN-AMP



Op Amp Applications, Chapter 2

2.16

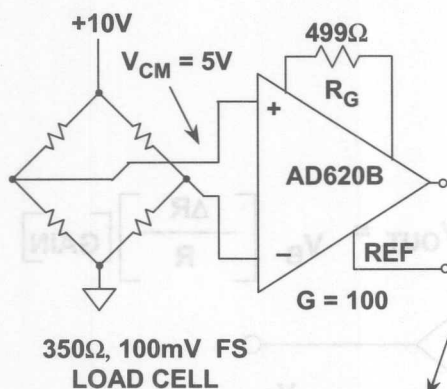
GENERALIZED BRIDGE AMPLIFIER USING AN IN-AMP



Op Amp Applications, Chapter 2

2.17

AD620B BRIDGE AMPLIFIER DC ERROR BUDGET

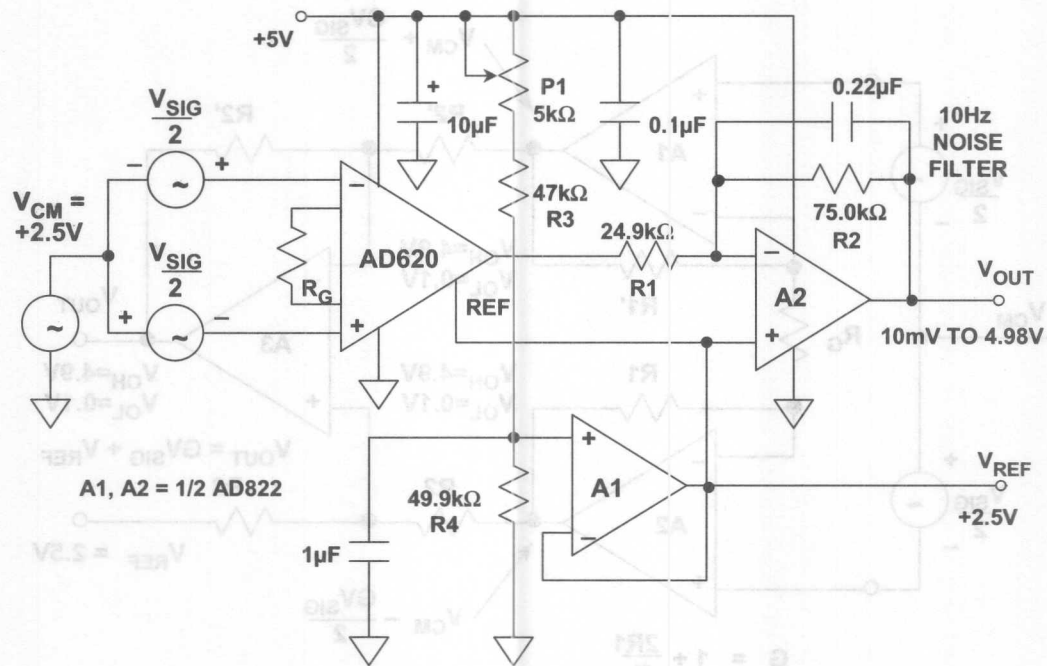


AD620B SPECS @ +25°C, ±15V
 $V_{OSI} + V_{OSO}/G = 55\mu\text{V max}$
 $I_{OS} = 0.5\text{nA max}$
 Gain Error = 0.15%
 Gain Nonlinearity = 40ppm
 0.1Hz to 10Hz Noise = 280nVp-p
 CMR = 120dB @ 60Hz

MAXIMUM ERROR CONTRIBUTION, +25°C
 FULLSCALE: $V_{IN} = 100\text{mV}$, $V_{OUT} = 10\text{V}$

V_{OS}	$55\mu\text{V} \div 100\text{mV}$	550ppm
I_{OS}	$350\Omega \times 0.5\text{nA} \div 100\text{mV}$	1.8ppm
Gain Error	0.15%	1500ppm
Gain Nonlinearity	40ppm	40ppm
CMR Error	120dB $1\text{ppm} \times 5\text{V} \div 100\text{mV}$	50ppm
0.1Hz to 10Hz 1/f Noise	$280\text{nV} \div 100\text{mV}$	2.8ppm
Total Unadjusted Error	≈ 9 Bits Accurate	2145ppm
Resolution Error	≈ 14 Bits Accurate	42.8ppm

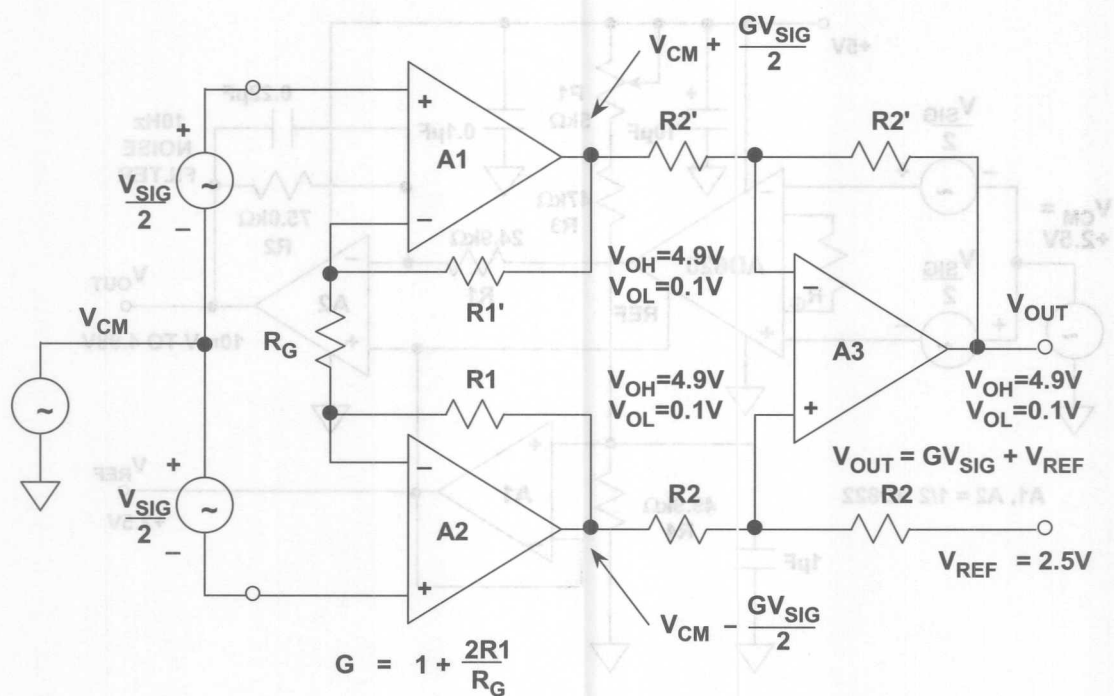
A PRECISION SINGLE-SUPPLY COMPOSITE IN-AMP WITH RAIL-TO-RAIL OUTPUT



Op Amp Applications, Chapter 2

2.19

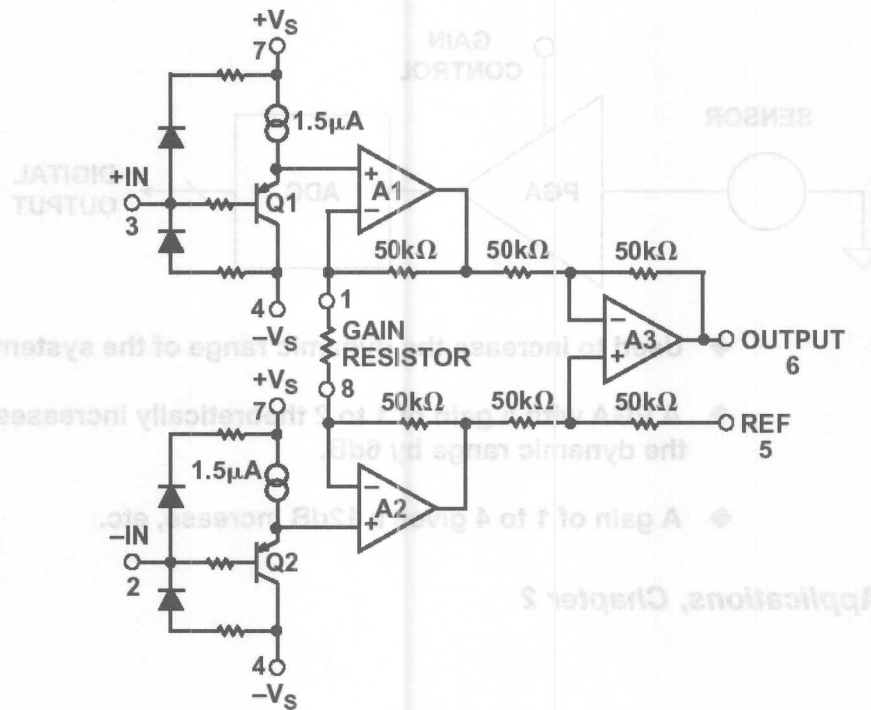
THREE OP AMP IN-AMP SINGLE +5V SUPPLY RESTRICTIONS



Op Amp Applications, Chapter 2

2.20

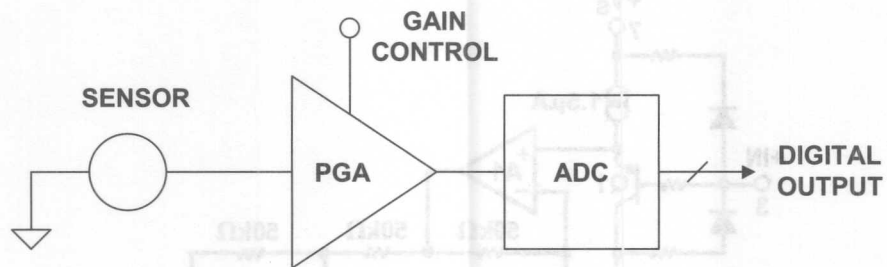
AD623 SINGLE-SUPPLY THREE OP-AMP IN-AMP ARCHITECTURE



Op Amp Applications, Chapter 2

2.21

PGAs IN DATA ACQUISITION SYSTEMS

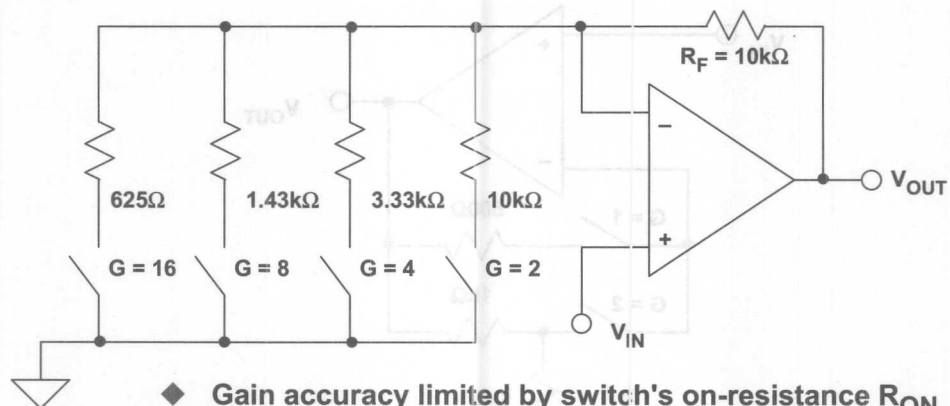


- ◆ Used to increase the dynamic range of the system
- ◆ A PGA with a gain of 1 to 2 theoretically increases the dynamic range by 6dB.
- ◆ A gain of 1 to 4 gives a 12dB increase, etc.

Op Amp Applications, Chapter 2

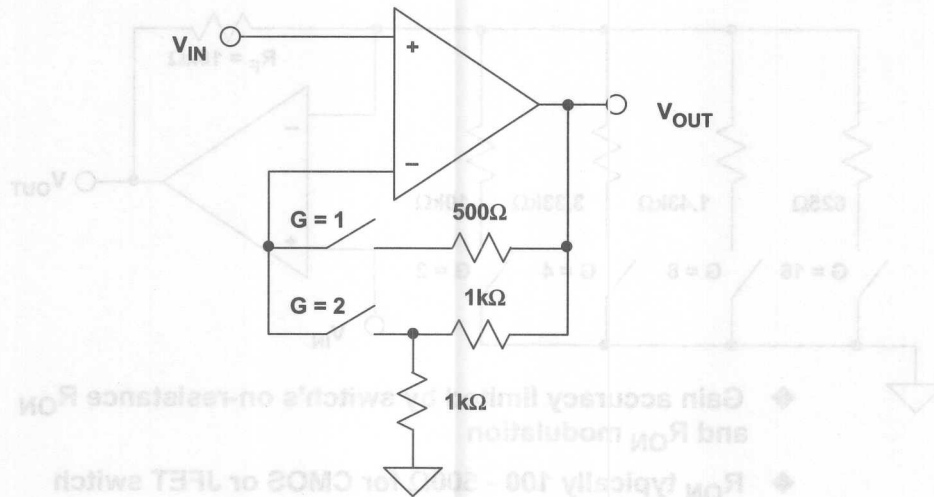
2.22

A POORLY DESIGNED PGA



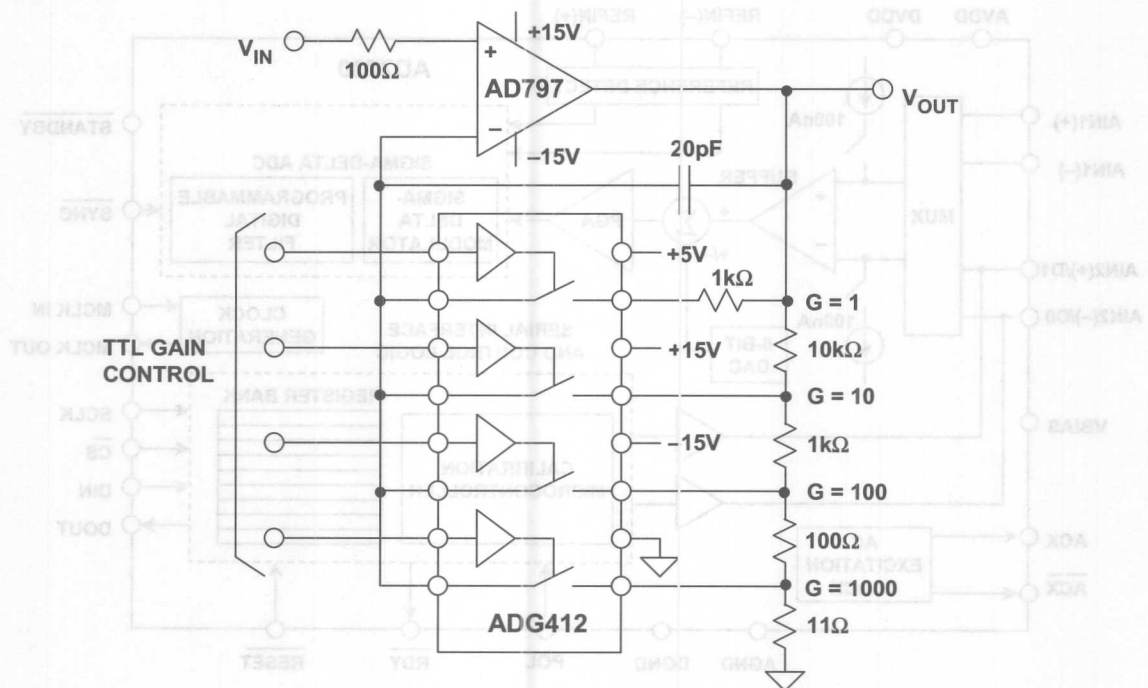
- ◆ Gain accuracy limited by switch's on-resistance R_{ON} and R_{ON} modulation
- ◆ R_{ON} typically 100 - 500 Ω for CMOS or JFET switch
- ◆ Even for $R_{ON} = 25\Omega$, there is a 2.4% gain error for $G = 16$
- ◆ R_{ON} drift over temperature limits accuracy
- ◆ Must use very low R_{ON} switches (relays)

ALTERNATE PGA CONFIGURATION MINIMIZES THE EFFECTS OF R_{ON}



- ◆ R_{ON} is not in series with gain setting resistors
- ◆ R_{ON} is small compared to input impedance
- ◆ Only slight offset errors occur due to bias current flowing through the switches

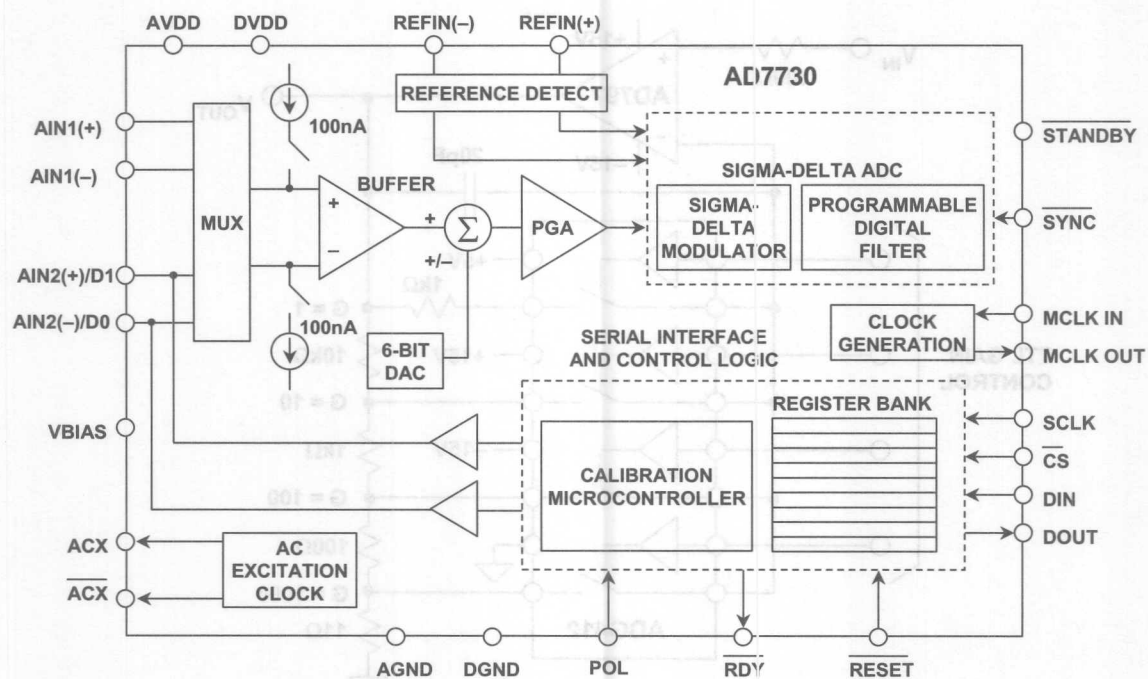
A VERY LOW NOISE PGA USING THE AD797 AND THE ADG412



Op Amp Applications, Chapter 2

2.25

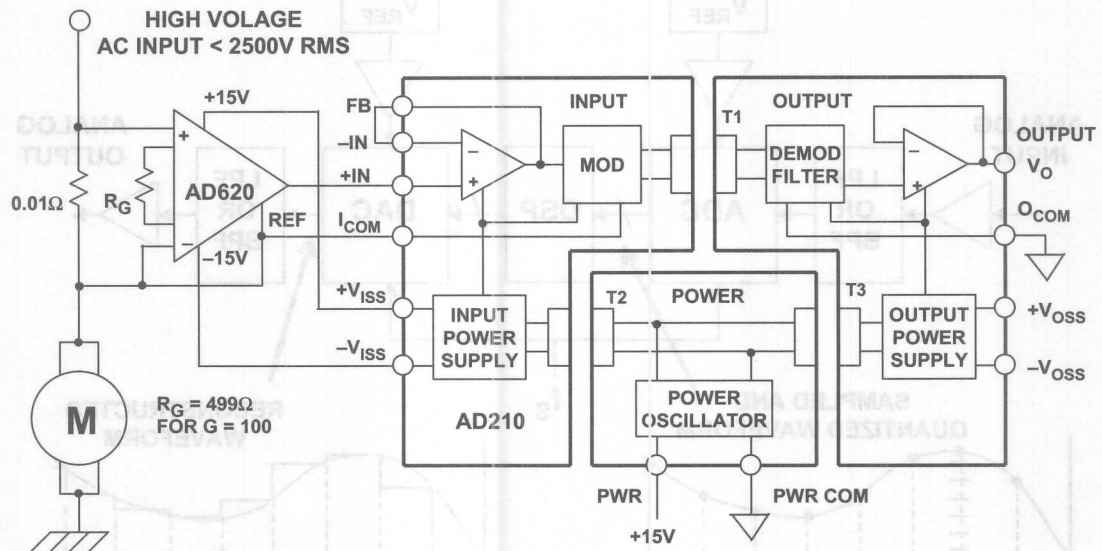
AD7730 SIGMA-DELTA MEASUREMENT ADC WITH ON-CHIP PGA



Op Amp Applications, Chapter 2

2.26

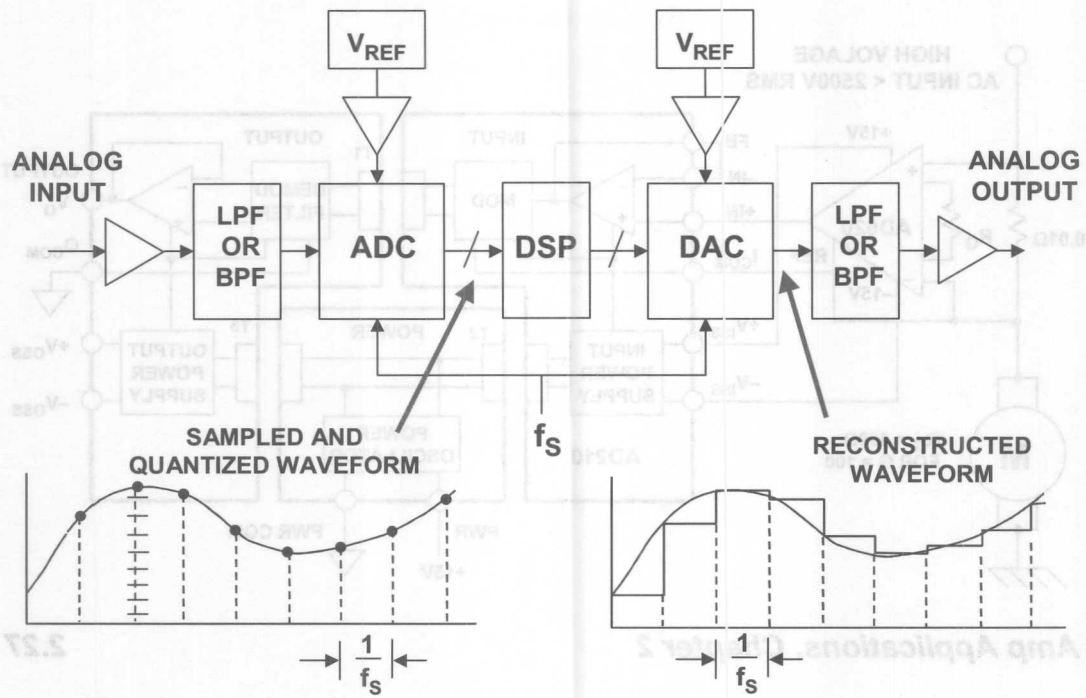
MOTOR CONTROL CURRENT SENSING USING AN ISOLATION AMPLIFIER



Op Amp Applications, Chapter 2

2.27

A TYPICAL SAMPLED DATA SYSTEM SHOWING APPLICATIONS OF OP AMPS



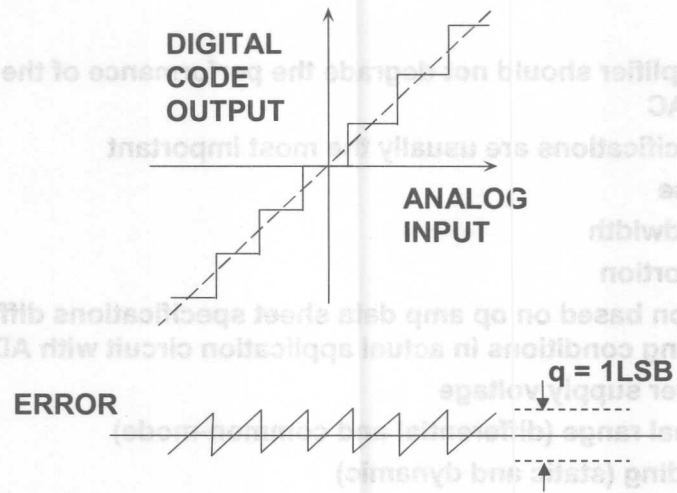
Op Amp Applications, Chapter 3

2.28

GENERAL OP AMP SELECTION CRITERIA FOR USE WITH DATA CONVERTERS

- ◆ The amplifier should not degrade the performance of the ADC/DAC
- ◆ AC specifications are usually the most important
 - Noise
 - Bandwidth
 - Distortion
- ◆ Selection based on op amp data sheet specifications difficult due to varying conditions in actual application circuit with ADC/DAC:
 - Power supply voltage
 - Signal range (differential and common-mode)
 - Loading (static and dynamic)
 - Gain
- ◆ Parametric search engines may be useful
- ◆ ADC/DAC data sheets often recommend op amps (but may not include newly released products)

IDEAL N-BIT ADC QUANTIZATION NOISE



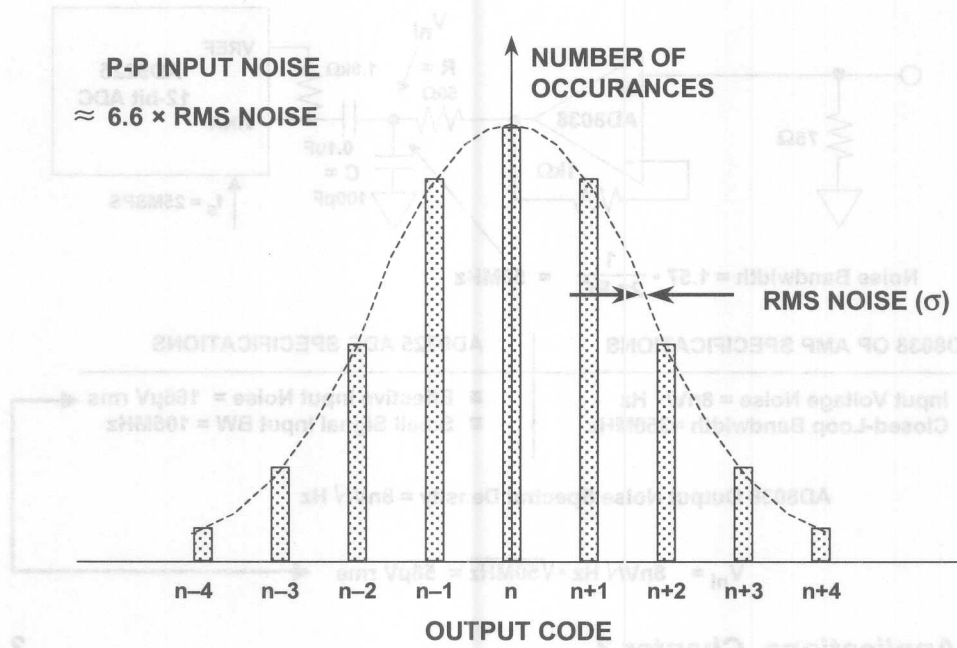
$$\text{RMS ERROR} = q/\sqrt{12}$$

$$\text{SNR} = 6.02N + 1.76\text{dB} + 10\log\left[\frac{f_s}{2 \cdot \text{BW}}\right] \quad \text{FOR FS SINEWAVE}$$

Op Amp Applications, Chapter 3

Op Amp Applications, Chapter 3 2.30

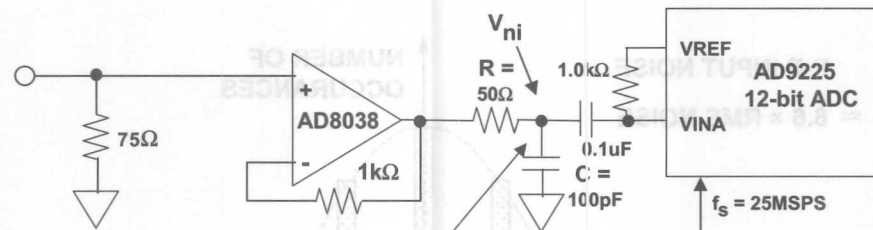
EFFECT OF INPUT-REFERRED NOISE ON ADC "GROUNDED INPUT" HISTOGRAM



Op Amp Applications, Chapter 3

2.31

NOISE CALCULATIONS FOR AD8038 OP AMP DRIVING AD9225 12-BIT, 25MSPS ADC



$$\text{Noise Bandwidth} = 1.57 \cdot \frac{1}{2\pi RC} = 50\text{MHz}$$

AD8038 OP AMP SPECIFICATIONS

- Input Voltage Noise = $8\text{nV}/\sqrt{\text{Hz}}$
- Closed-Loop Bandwidth = 350MHz

AD9225 ADC SPECIFICATIONS

- Effective Input Noise = $166\mu\text{V rms}$
- Small Signal Input BW = 105MHz

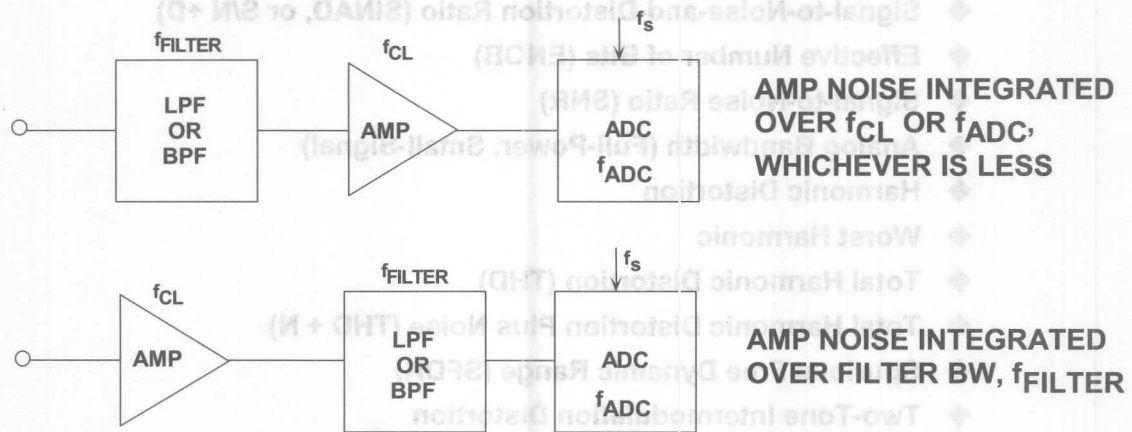
AD8038 Output Noise Spectral Density = $8\text{nV}/\sqrt{\text{Hz}}$

$$V_{ni} = 8\text{nV}/\sqrt{\text{Hz}} \cdot \sqrt{50\text{MHz}} = 56\mu\text{V rms}$$

Op Amp Applications, Chapter 3

2.32

POSITIONING THE ANTIALIASING FILTER TO REDUCE THE EFFECTS OF THE OP AMP NOISE



IN GENERAL, $f_{\text{FILTER}} < \frac{f_s}{2} \ll f_{\text{ADC}} < f_{\text{CL}}$

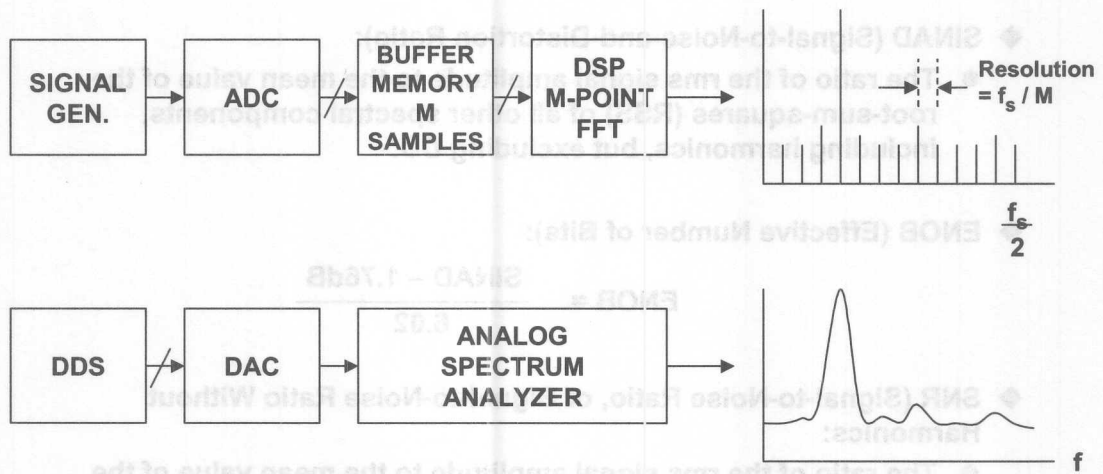
POPULAR CONVERTER DYNAMIC PERFORMANCE SPECIFICATIONS

- ◆ Signal-to-Noise-and-Distortion Ratio (SINAD, or $S/N + D$)
- ◆ Effective Number of Bits (ENOB)
- ◆ Signal-to-Noise Ratio (SNR)
- ◆ Analog Bandwidth (Full-Power, Small-Signal)
- ◆ Harmonic Distortion
- ◆ Worst Harmonic
- ◆ Total Harmonic Distortion (THD)
- ◆ Total Harmonic Distortion Plus Noise (THD + N)
- ◆ Spurious Free Dynamic Range (SFDR)
- ◆ Two-Tone Intermodulation Distortion
- ◆ Multi-tone Intermodulation Distortion

Op Amp Applications, Chapter 3

2.34

TEST SETUPS FOR MEASURING ADC AND DAC PERFORMANCE



Op Amp Applications, Chapter 3

2.35

SINAD, ENOB, AND SNR DEFINITIONS

◆ **SINAD (Signal-to-Noise-and-Distortion Ratio):**

- The ratio of the rms signal amplitude to the mean value of the root-sum-squares (RSS) of all other spectral components, including harmonics, but excluding DC.

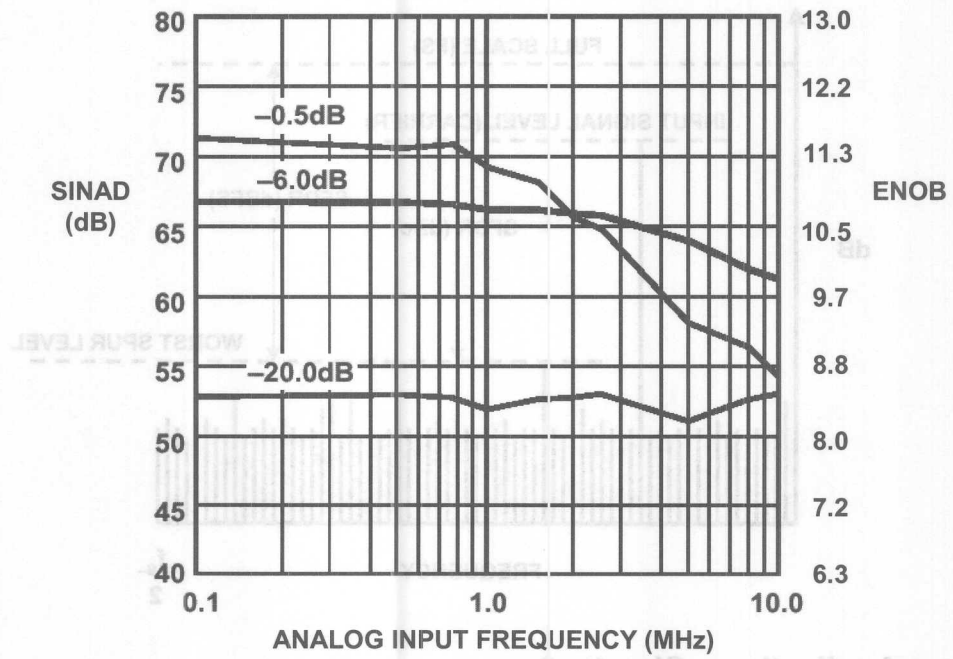
◆ **ENOB (Effective Number of Bits):**

$$\text{ENOB} = \frac{\text{SINAD} - 1.76\text{dB}}{6.02}$$

◆ **SNR (Signal-to-Noise Ratio, or Signal-to-Noise Ratio Without Harmonics):**

- The ratio of the rms signal amplitude to the mean value of the root-sum-squares (RSS) of all other spectral components, excluding the first 5 harmonics and DC

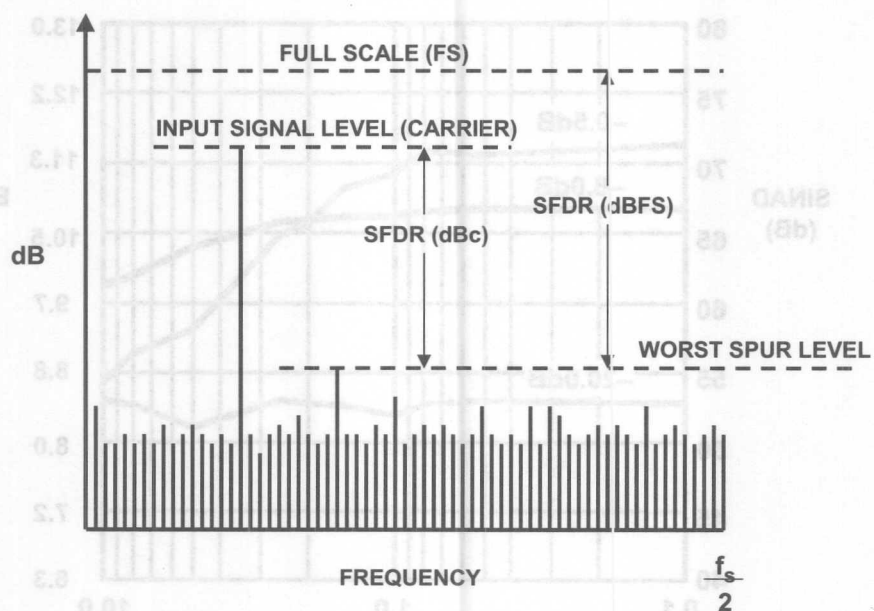
AD9220 12-BIT, 10MSPS ADC SINAD AND ENOB FOR VARIOUS INPUT SIGNAL LEVELS



Op Amp Applications, Chapter 3

2.37

SPURIOUS FREE DYNAMIC RANGE (SFDR)



Op Amp Applications, Chapter 3

2.38

SOME GENERAL OP AMP REQUIREMENTS IN ADC DRIVER APPLICATIONS

- ◆ Minimize degradation of ADC / DAC performance specifications
- ◆ Fast settling to ADC/DAC transient
- ◆ High bandwidth
- ◆ Low noise
- ◆ Low distortion
- ◆ Low power

- ◆ Note: Op amp performance must be measured under identical conditions as encountered in ADC / DAC application
 - Gain setting resistors
 - Input source impedance, output load impedance
 - Input / output signal voltage range
 - Input signal frequency
 - Input / output common-mode level
 - Power supply voltage (single or dual supply)
 - Transient loading

KEY DC AND AC OP AMP SPECIFICATIONS FOR ADC APPLICATIONS

◆ DC

- Offset, offset drift
- Input bias current
- Open loop gain
- Integral linearity
- 1/f noise (voltage and current)

◆ AC (Highly application dependent!)

- Wideband noise (voltage and current)
- Small and Large Signal Bandwidth
- Harmonic Distortion
- Total Harmonic Distortion (THD)
- Total Harmonic Distortion + Noise (THD + N)
- Spurious Free Dynamic Range (SFDR)
- Third Order Intermodulation Distortion
- Third Order Intercept Point

Op Amp Applications, Chapter 3

2.40

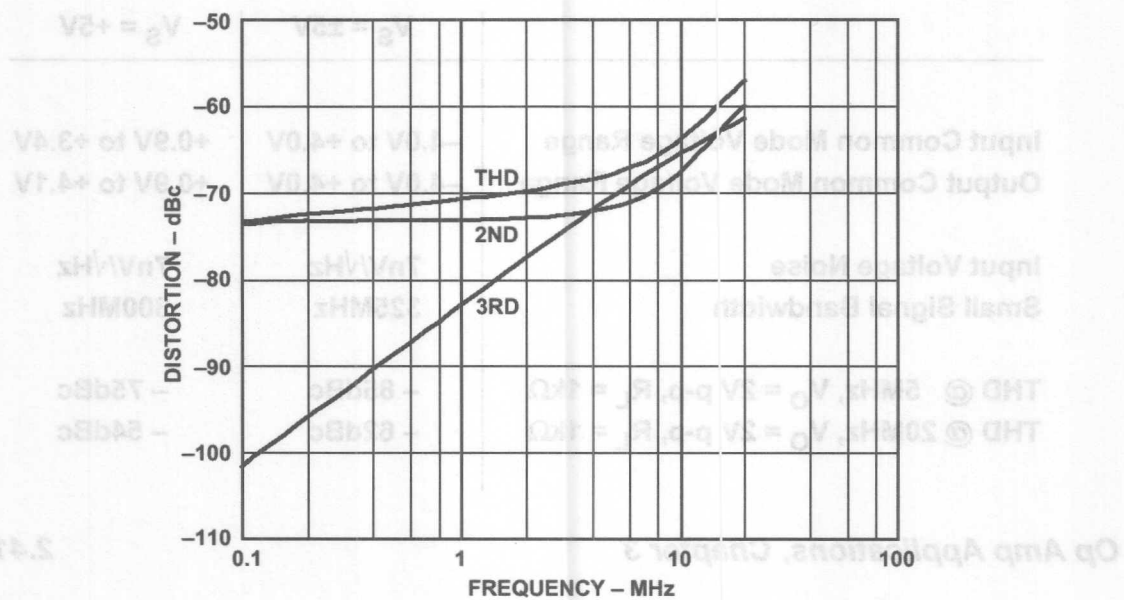
KEY SPECIFICATIONS FOR THE AD8057/8058 OP AMP, $G = +1$

	$V_S = \pm 5V$	$V_S = +5V$
Input Common Mode Voltage Range	-4.0V to +4.0V	+0.9V to +3.4V
Output Common Mode Voltage Range	-4.0V to +4.0V	+0.9V to +4.1V
Input Voltage Noise	7nV/ $\sqrt{\text{Hz}}$	7nV/ $\sqrt{\text{Hz}}$
Small Signal Bandwidth	325MHz	300MHz
THD @ 5MHz, $V_O = 2V$ p-p, $R_L = 1k\Omega$	- 85dBc	- 75dBc
THD @ 20MHz, $V_O = 2V$ p-p, $R_L = 1k\Omega$	- 62dBc	- 54dBc

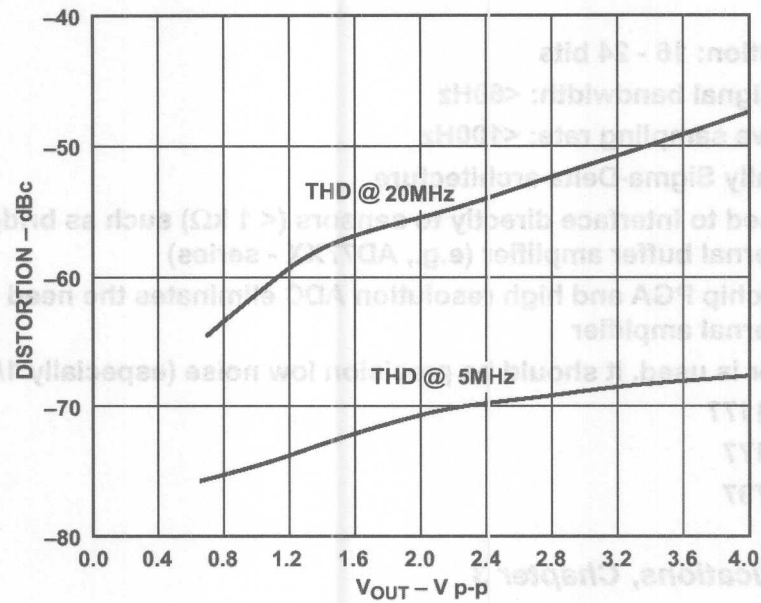
Op Amp Applications, Chapter 3

2.41

AD8057/8058 OP AMP DISTORTION VS. FREQUENCY FOR $G = +1$, $V_S = \pm 5V$, $V_O = 2V_{p-p}$, $R_L = 150\Omega$



AD8057/8058 OP AMP DISTORTION VS. OUTPUT SIGNAL LEVEL FOR $G = +1$, $V_S = \pm 5V$, $R_L = 150\Omega$

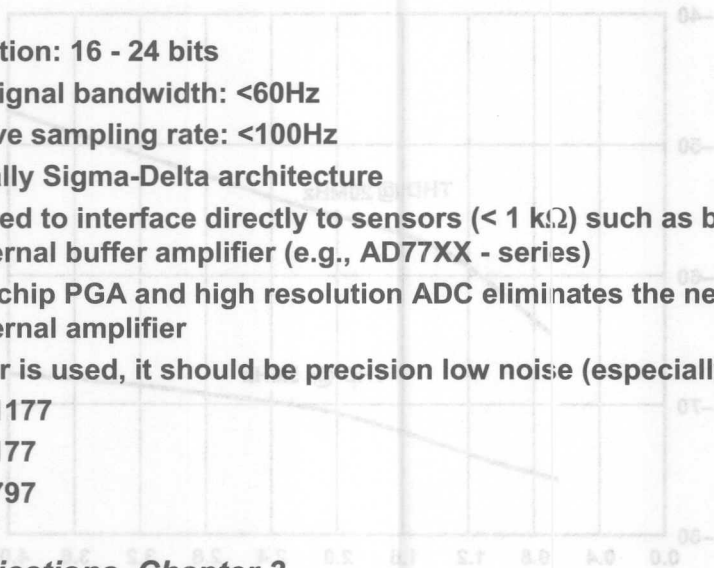


Op Amp Applications, Chapter 3

2.43

CHARACTERISTICS OF AD77XX-FAMILY HIGH RESOLUTION SIGMA-DELTA MEASUREMENT ADCs

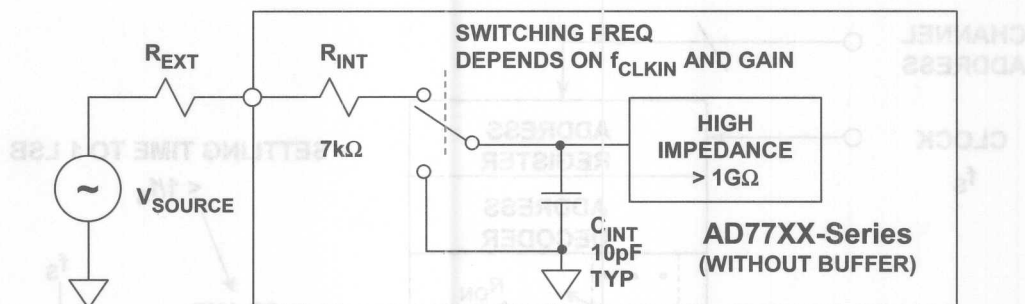
- ◆ Resolution: 16 - 24 bits
- ◆ Input signal bandwidth: <60Hz
- ◆ Effective sampling rate: <100Hz
- ◆ Generally Sigma-Delta architecture
- ◆ Designed to interface directly to sensors (< 1 k Ω) such as bridges with no external buffer amplifier (e.g., AD77XX - series)
 - On-chip PGA and high resolution ADC eliminates the need for external amplifier
- ◆ If buffer is used, it should be precision low noise (especially 1/f noise)
 - OP1177
 - OP177
 - AD797



Op Amp Applications, Chapter 3

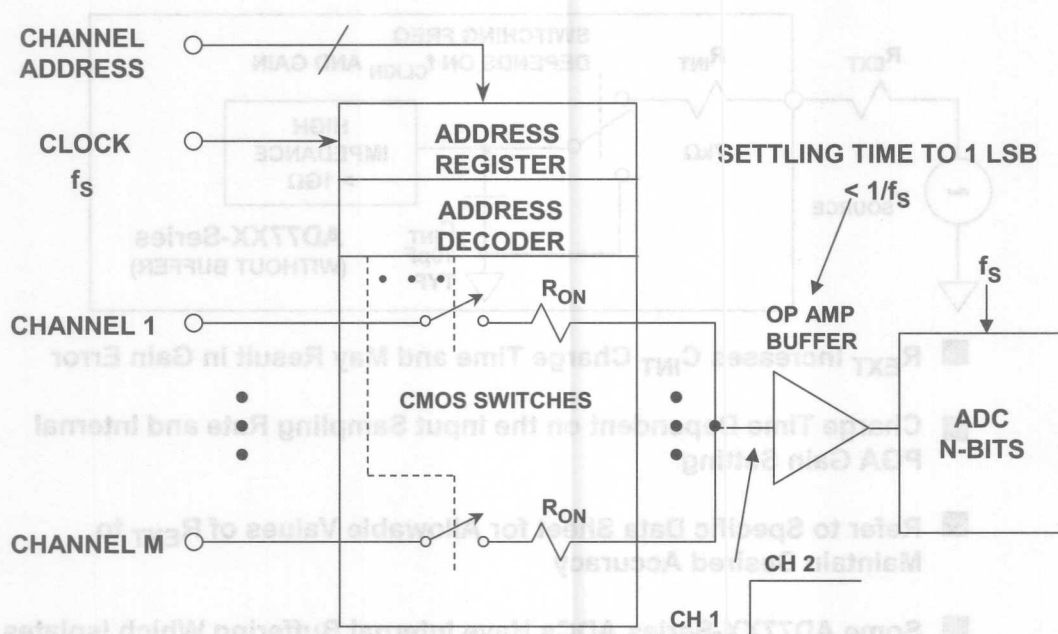
2.44

DRIVING UNBUFFERED AD77XX-SERIES $\Sigma\Delta$ ADC INPUTS



- R_{EXT} Increases C_{INT} Charge Time and May Result in Gain Error
- Charge Time Dependent on the Input Sampling Rate and Internal PGA Gain Setting
- Refer to Specific Data Sheet for Allowable Values of R_{EXT} to Maintain Desired Accuracy
- Some AD77XX-Series ADCs Have Internal Buffering Which Isolates Input from Switching Circuits

MULTIPLEXED DATA ACQUISITION SYSTEM REQUIRES FAST SETTLING OP AMP BUFFER

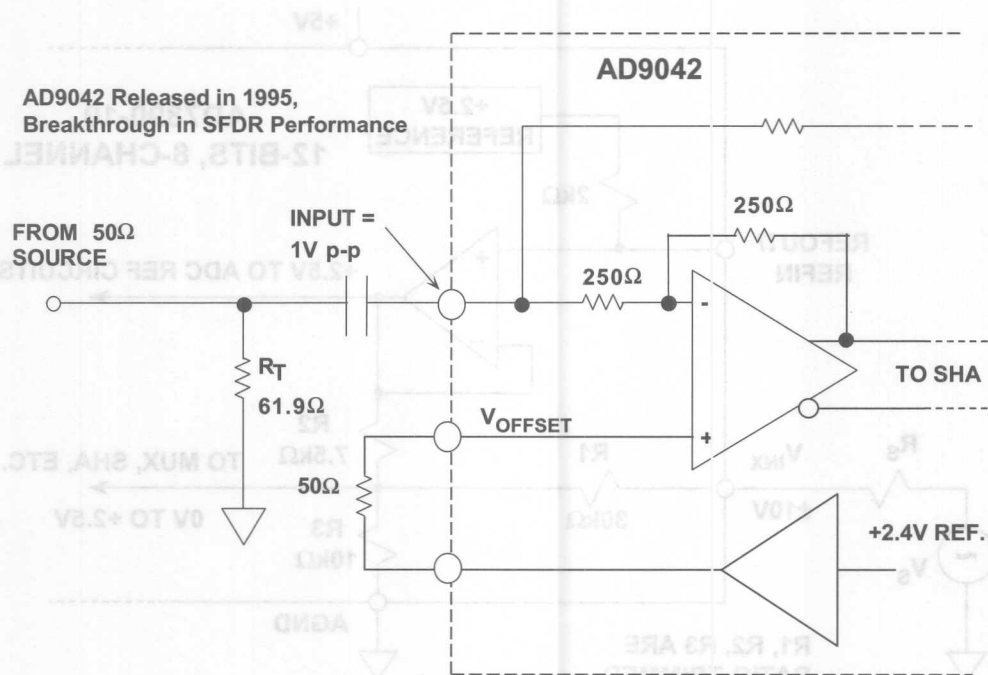


Op Amp Applications, Chapter 3

2.46



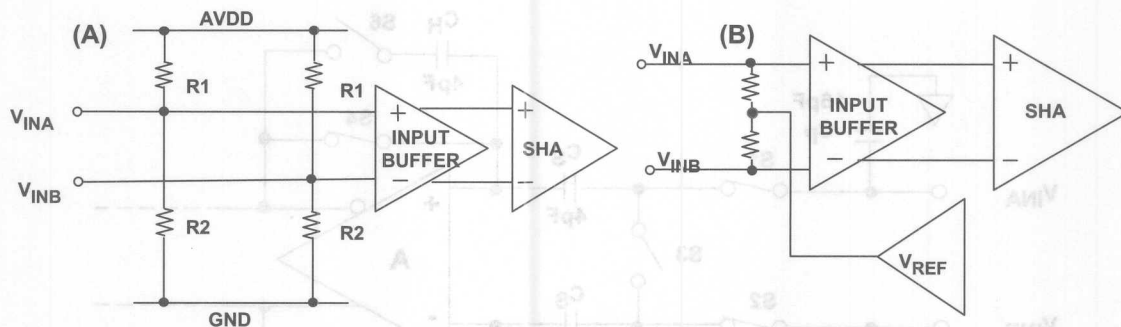
AD9042 12-BIT, 41MSPS ADC IS DESIGNED TO BE DRIVEN DIRECTLY FROM 50Ω SOURCE WITH NO EXTERNAL OP AMP



Op Amp Applications, Chapter 3

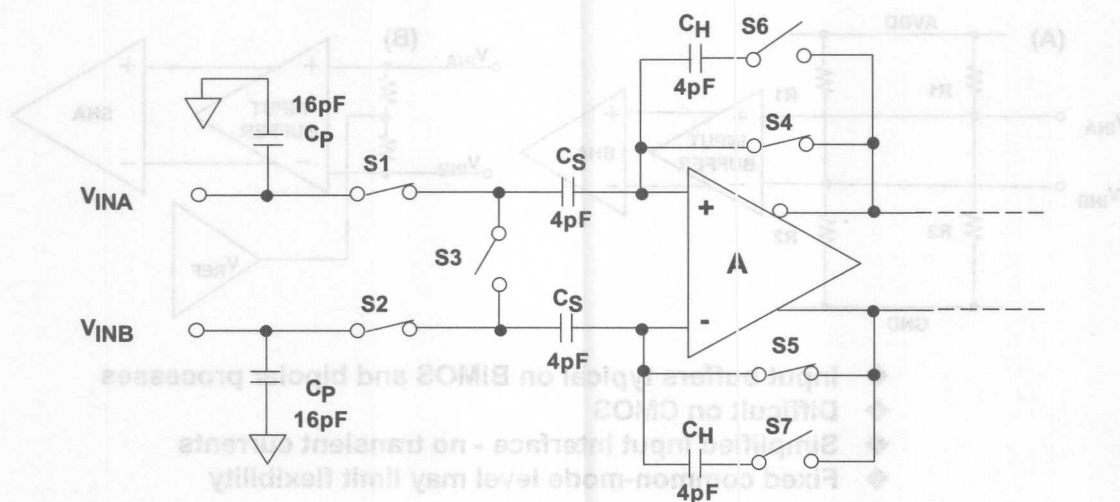
2.48

ADCs WITH BUFFERED DIFFERENTIAL INPUTS



- ◆ Input buffers typical on BiMOS and bipolar processes
- ◆ Difficult on CMOS
- ◆ Simplified input interface - no transient currents
- ◆ Fixed common-mode level may limit flexibility

SIMPLIFIED INPUT CIRCUIT FOR A TYPICAL SWITCHED CAPACITOR CMOS SAMPLE-AND-HOLD



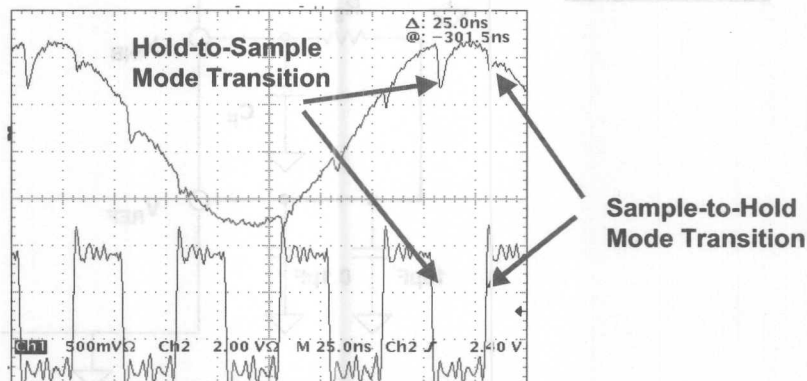
SWITCHES SHOWN IN TRACK MODE

Op Amp Applications, Chapter 3

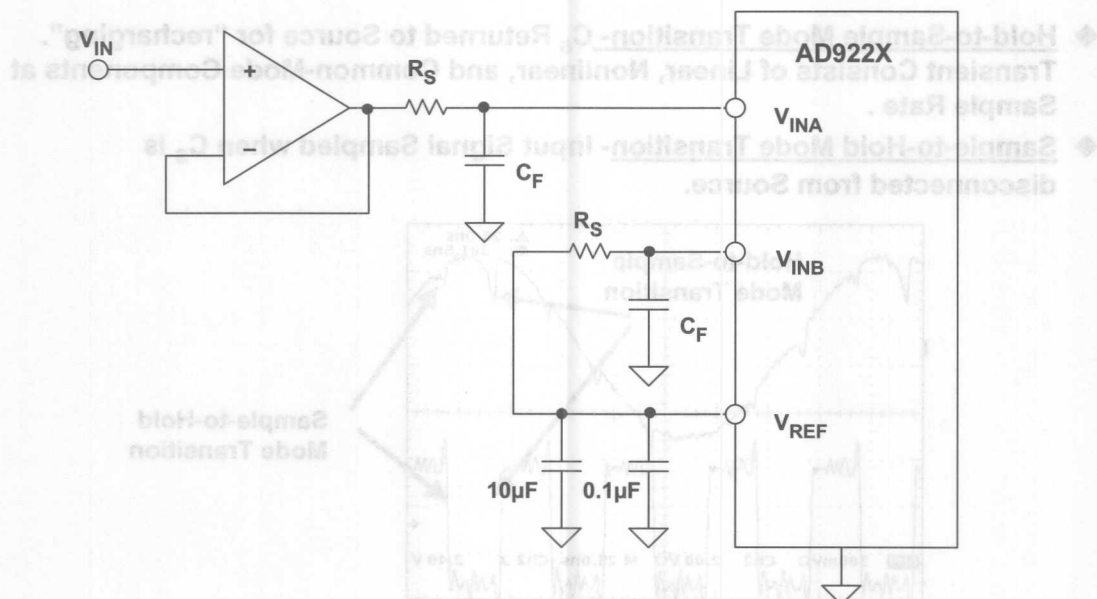
2.50

SINGLE-ENDED INPUT TRANSIENTS ON THE AD9225 12-BIT, 25MSPS CMOS ADC

- ◆ **Hold-to-Sample Mode Transition-** C_S Returned to Source for “recharging”. Transient Consists of Linear, Nonlinear, and Common-Mode Components at Sample Rate .
- ◆ **Sample-to-Hold Mode Transition-** Input Signal Sampled when C_S is disconnected from Source.



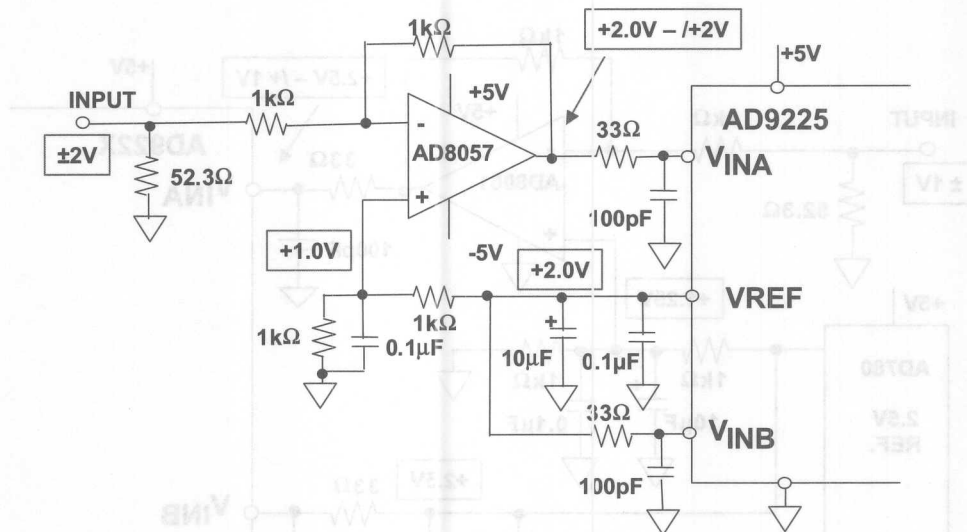
OPTIMIZING A SINGLE-ENDED SWITCHED CAPACITOR ADC INPUT DRIVE CIRCUIT



Op Amp Applications, Chapter 3

Op Amp Applications, Chapter 3 2.52

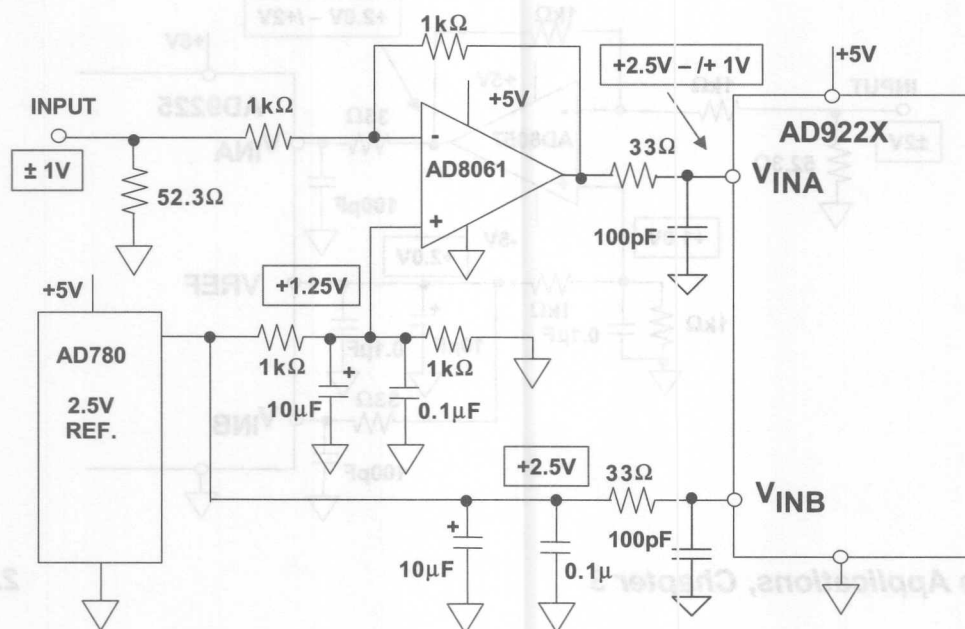
DC COUPLED SINGLE-ENDED LEVEL SHIFTER AND DRIVER FOR THE AD9225 12-BIT, 25MSPS CMOS ADC



Op Amp Applications, Chapter 3

2.53

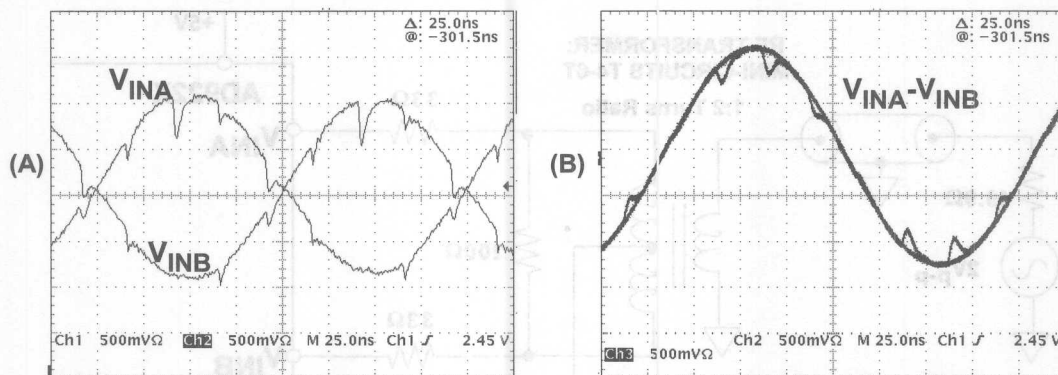
DIRECT-COUPLED SINGLE-SUPPLY LEVEL SHIFTER FOR DRIVING AD922X ADC INPUT



Op Amp Applications, Chapter 3

2.54

**SINGLE-ENDED (A) AND DIFFERENTIAL (B) INPUT TRANSIENTS OF
AD9225 12-BIT, 25MSPS CMOS SWITCHED CAPACITOR ADC**

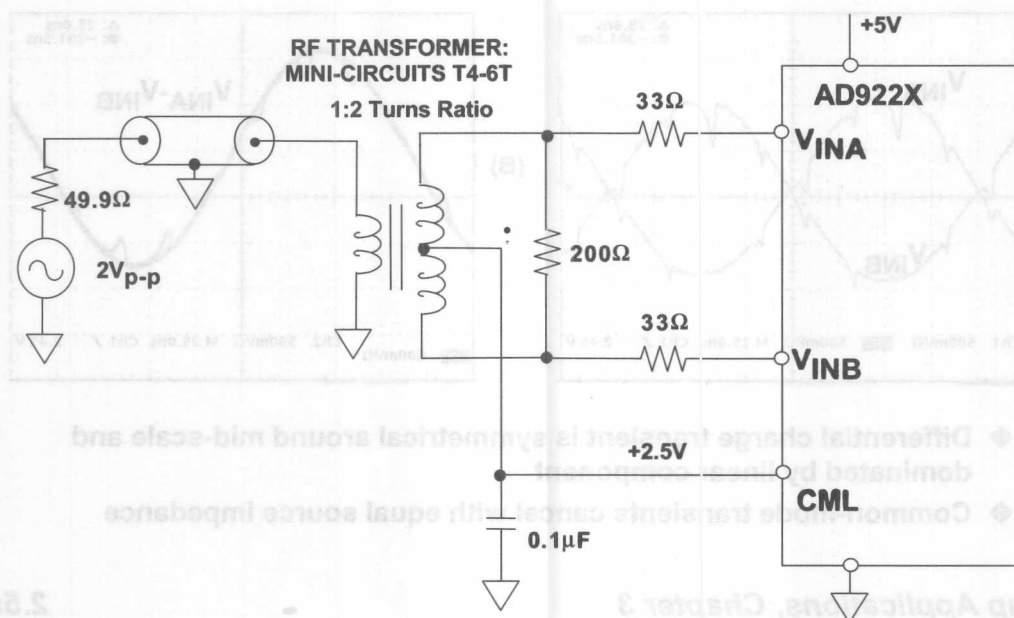


- ◆ Differential charge transient is symmetrical around mid-scale and dominated by linear component
- ◆ Common-mode transients cancel with equal source impedance

Op Amp Applications, Chapter 3

2.55

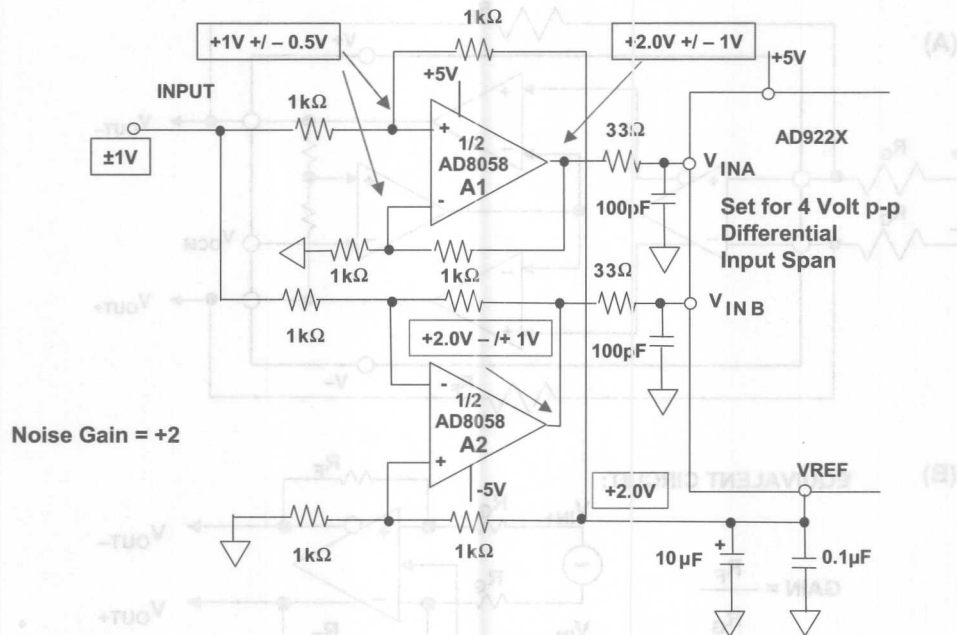
TRANSFORMER COUPLING INTO A DIFFERENTIAL INPUT ADC



Op Amp Applications, Chapter 3

2.56

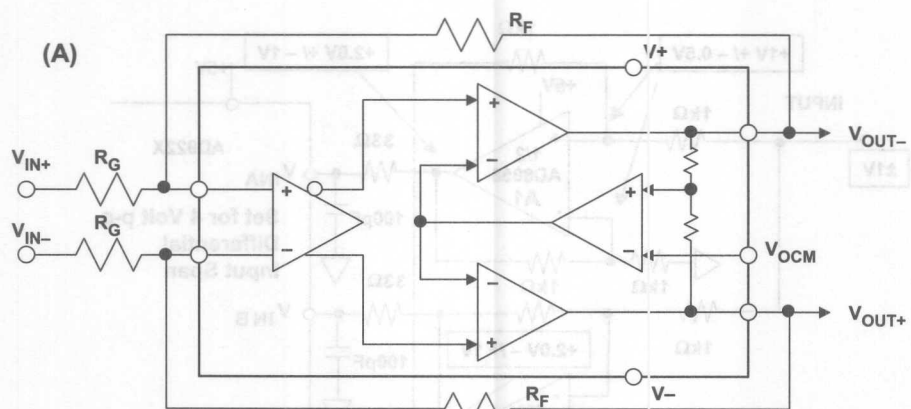
OP AMP SINGLE-ENDED TO DIFFERENTIAL DC COUPLED DRIVER WITH LEVEL SHIFTING



Op Amp Applications, Chapter 3

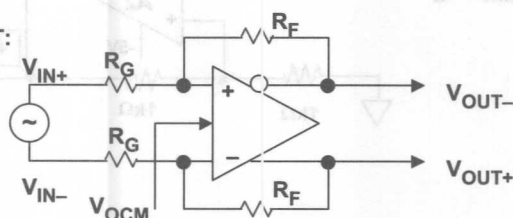
2.57

AD813X DIFFERENTIAL ADC DRIVER FUNCTIONAL DIAGRAM AND EQUIVALENT CIRCUIT

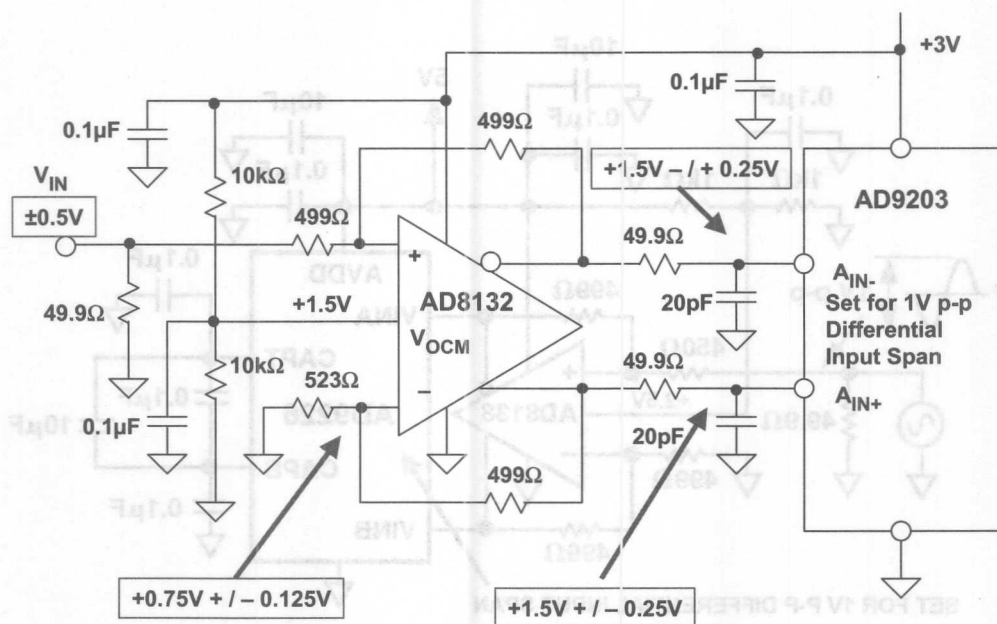


(B) EQUIVALENT CIRCUIT:

$$GAIN = \frac{R_F}{R_G}$$



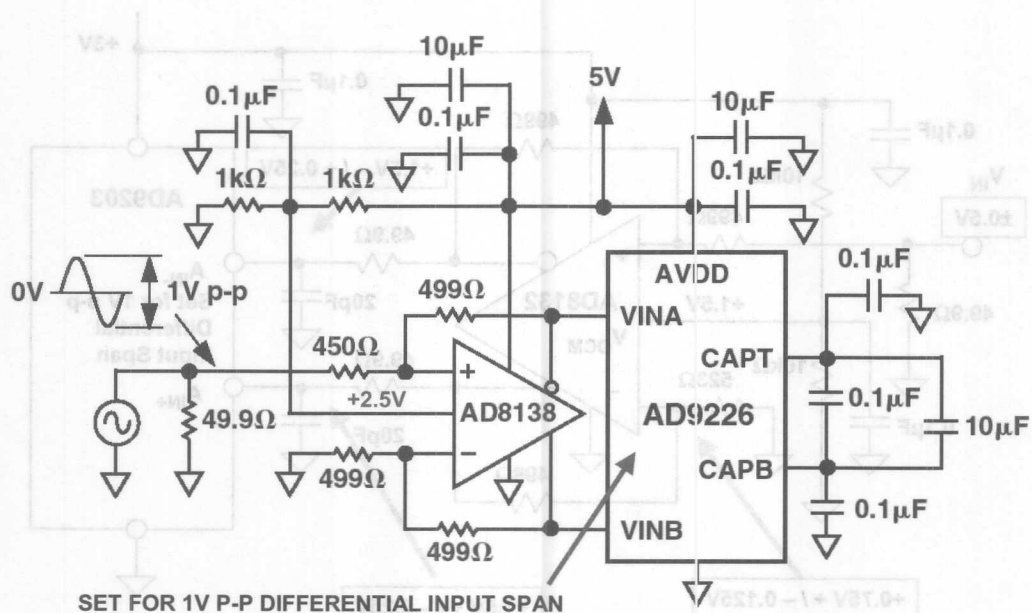
SINGLE-SUPPLY DIFFERENTIAL DRIVER CIRCUIT USING THE AD8132 AMPLIFIER AND THE AD9203 10-BIT, 40MSPS ADC



Op Amp Applications, Chapter 3

2.59

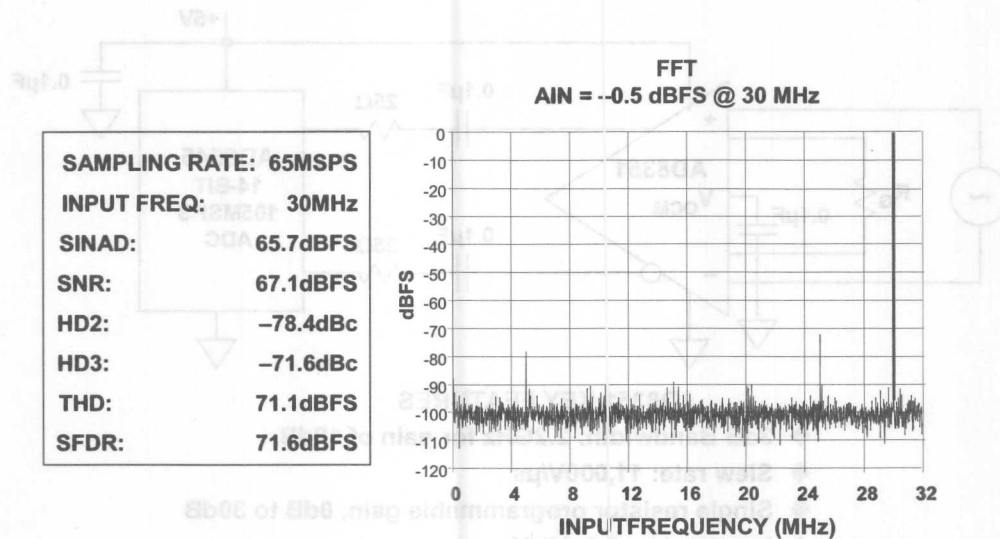
AD8138 DRIVING AD9226 12-BIT, 65MSPS CMOS ADC IN DIRECT-COUPLED SINGLE-SUPPLY APPLICATION



Op Amp Applications, Chapter 3

2.60

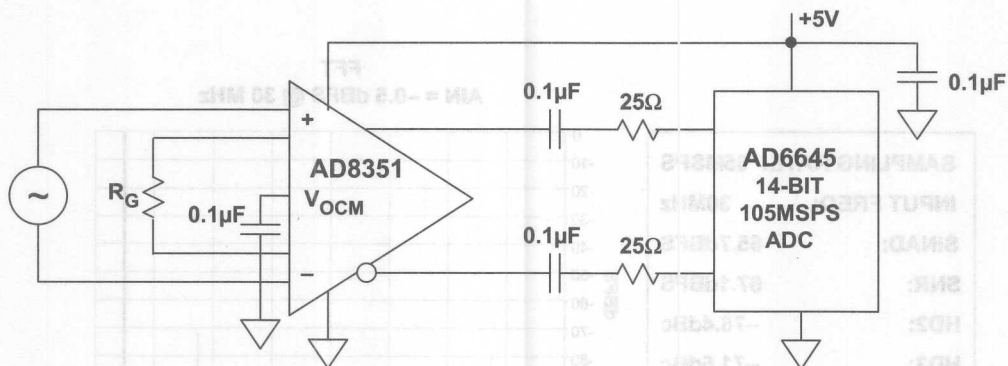
AD8138 DRIVING AD9226 ADC 1V DIFFERENTIAL INPUT SPAN, $f_s = 65\text{MSPS}$



Op Amp Applications, Chapter 3

2.61

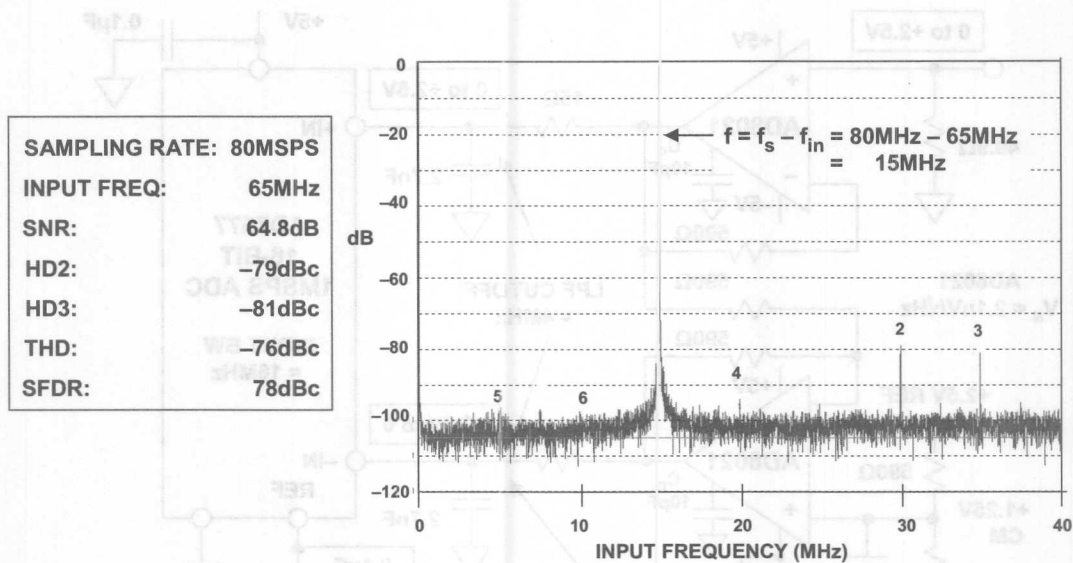
AD8351 LOW DISTORTION DIFFERENTIAL RF/IF AMPLIFIER APPLICATION



AD8351 KEY FEATURES

- ◆ 3dB Bandwidth: 2.2GHz for gain of 12dB
- ◆ Slew rate: 11,000V/µs
- ◆ Single resistor programmable gain, 0dB to 30dB
- ◆ Input noise: 2.3nV/√Hz
- ◆ Single supply: 3.3 to 5.5V
- ◆ Adjustable output common-mode voltage

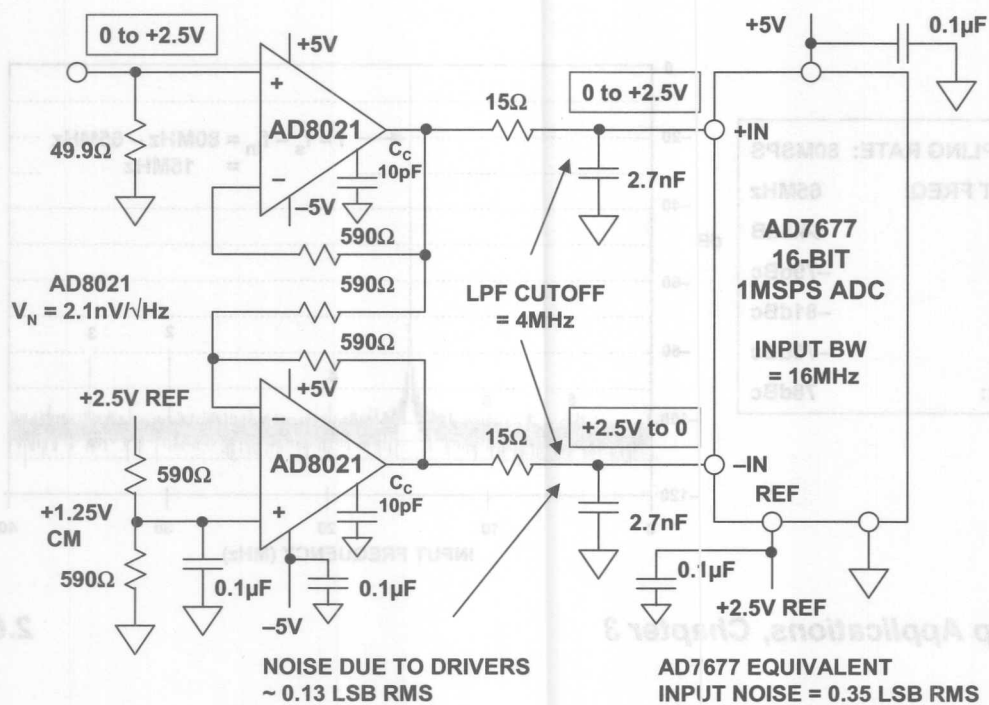
AD8351 DIFFERENTIAL ADC DRIVER PERFORMANCE WITH AD6645 ADC



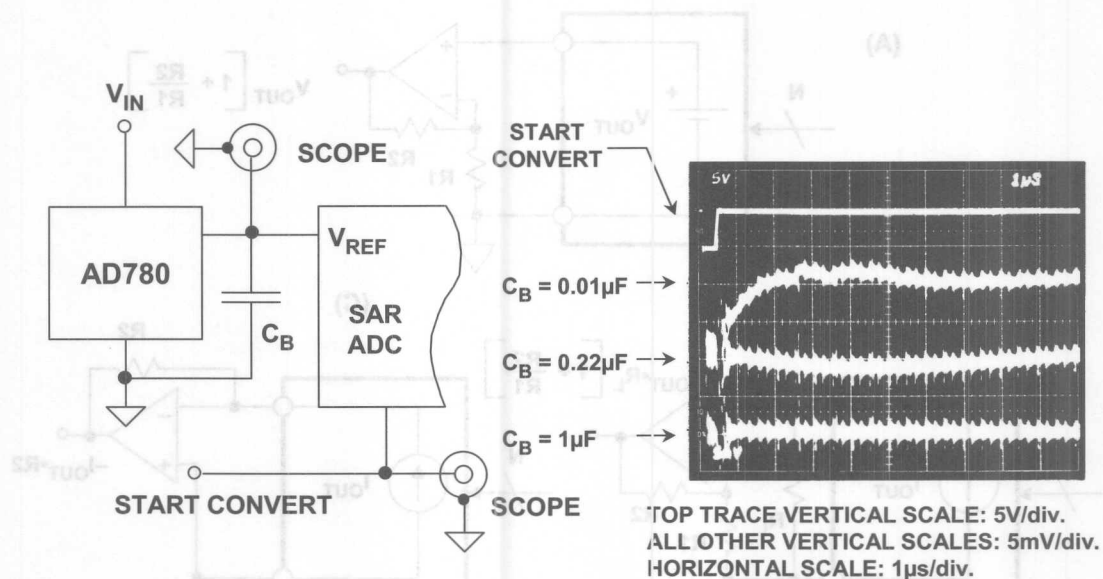
Op Amp Applications, Chapter 3

2.63

A TRUE 16-BIT ADC REQUIRES A TRUE 16-BIT DRIVER



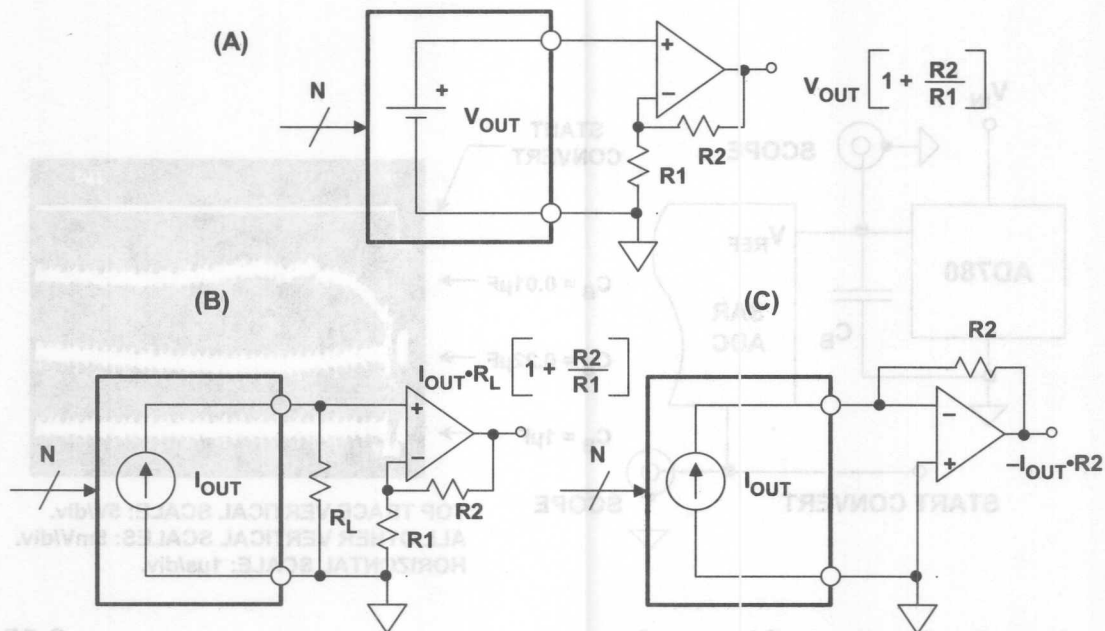
SAR ADCs PRESENT A DYNAMIC TRANSIENT LOAD TO THE REFERENCE



Op Amp Applications, Chapter 3

2.65

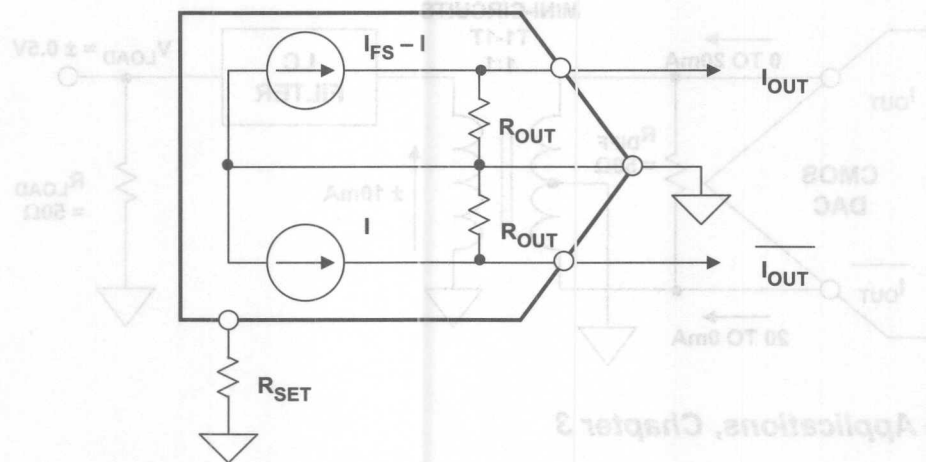
BUFFERING DAC OUTPUTS USING OP AMPS



Op Amp Applications, Chapter 3

2.66

GENERALIZED MODEL OF A HIGH SPEED DAC OUTPUT SUCH AS THE AD976X AND AD977X SERIES

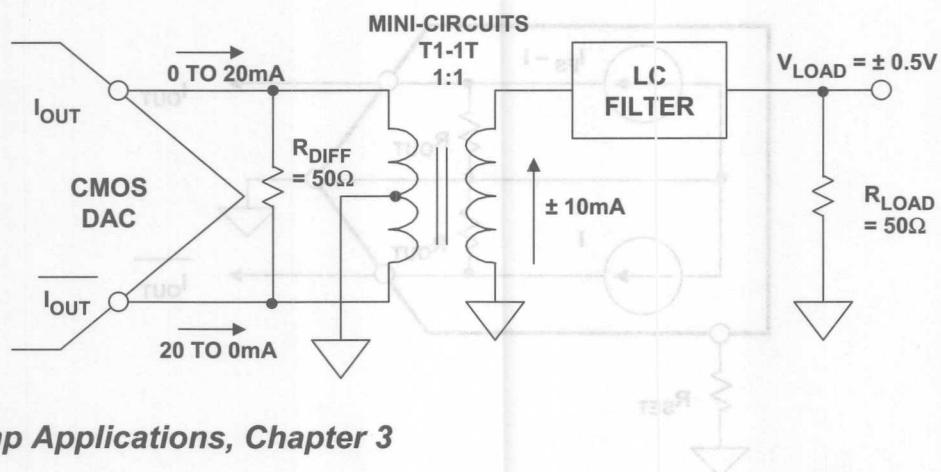


- ◆ I_{FS} 2 - 20mA typical
- ◆ Bipolar or BiCMOS DACs sink current, $R_{OUT} < 500\Omega$
- ◆ CMOS DACs source current, $R_{OUT} > 100k\Omega$
- ◆ Output compliance voltage $< \pm 1V$ for best performance

Op Amp Applications, Chapter 3

2.67

DIFFERENTIAL TRANSFORMER COUPLING



Op Amp Applications, Chapter 3

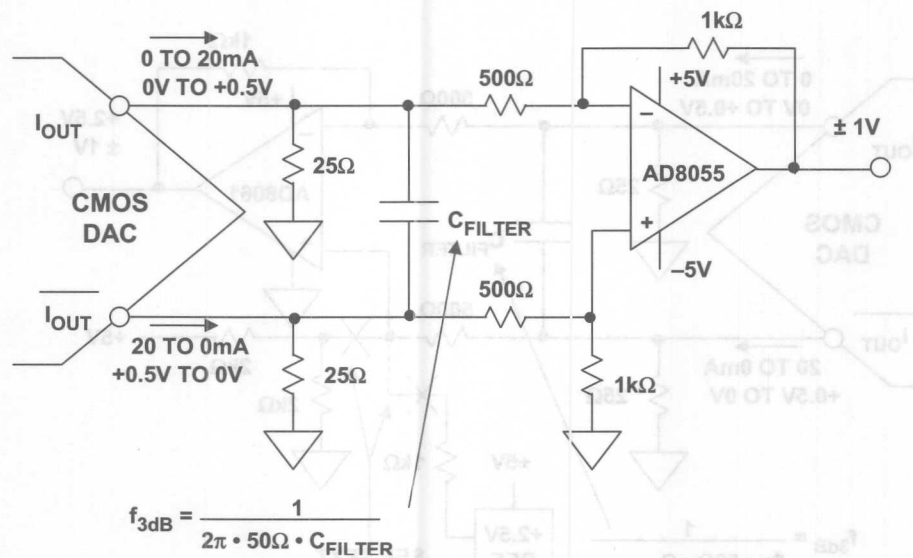
2.68

- ◆ Output compliance voltage $< \pm 1V$ for best performance
- ◆ CMOS DACs source current, $R_{OUT} > 100k\Omega$
- ◆ Bipolar or BiCMOS DACs sink current, $R_{OUT} < 500\Omega$
- ◆ $I_{FS} = 20mA$ typical

2.67

Op Amp Applications, Chapter 3

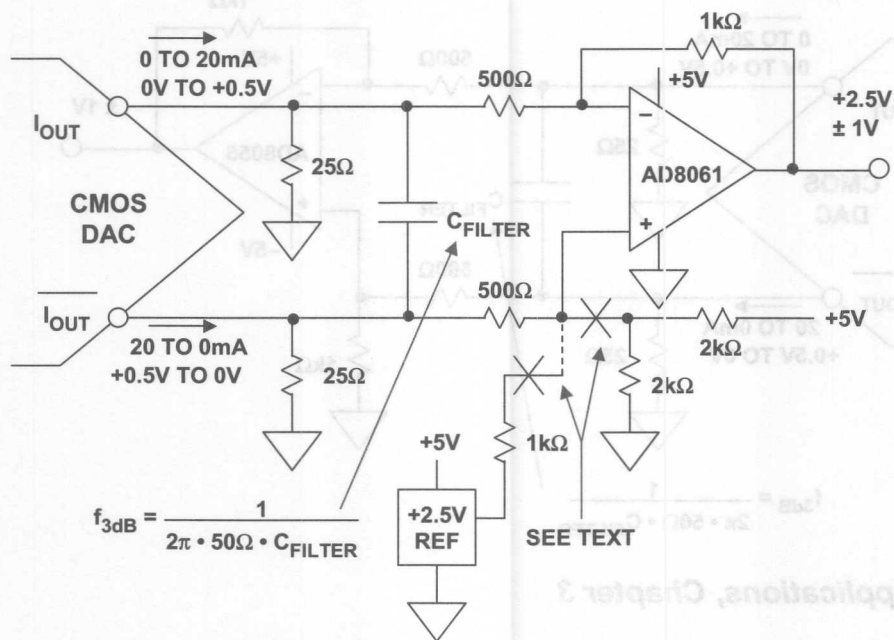
DIFFERENTIAL DC COUPLED USING A DUAL SUPPLY OP AMP



Op Amp Applications, Chapter 3

2.69

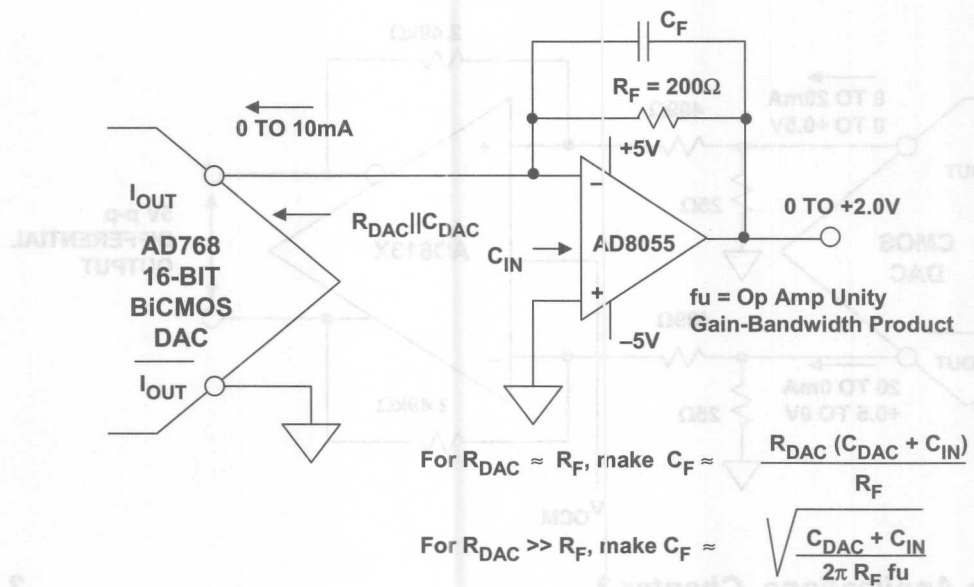
DIFFERENTIAL DC COUPLED W/ SINGLE SUPPLY OP AMP



Op Amp Applications, Chapter 3

2.70

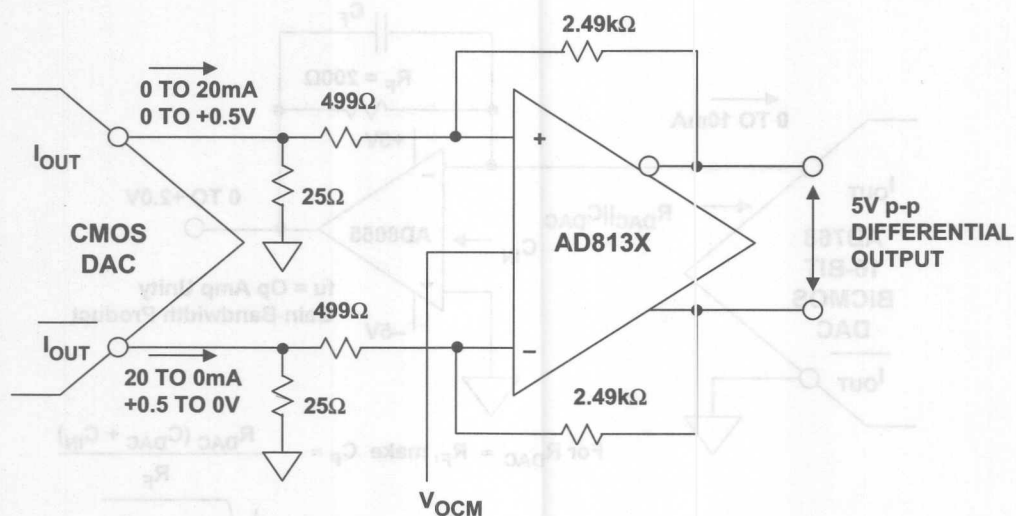
SINGLE-ENDED CURRENT-TO-VOLTAGE OP AMP INTERFACE



Op Amp Applications, Chapter 3

2.71

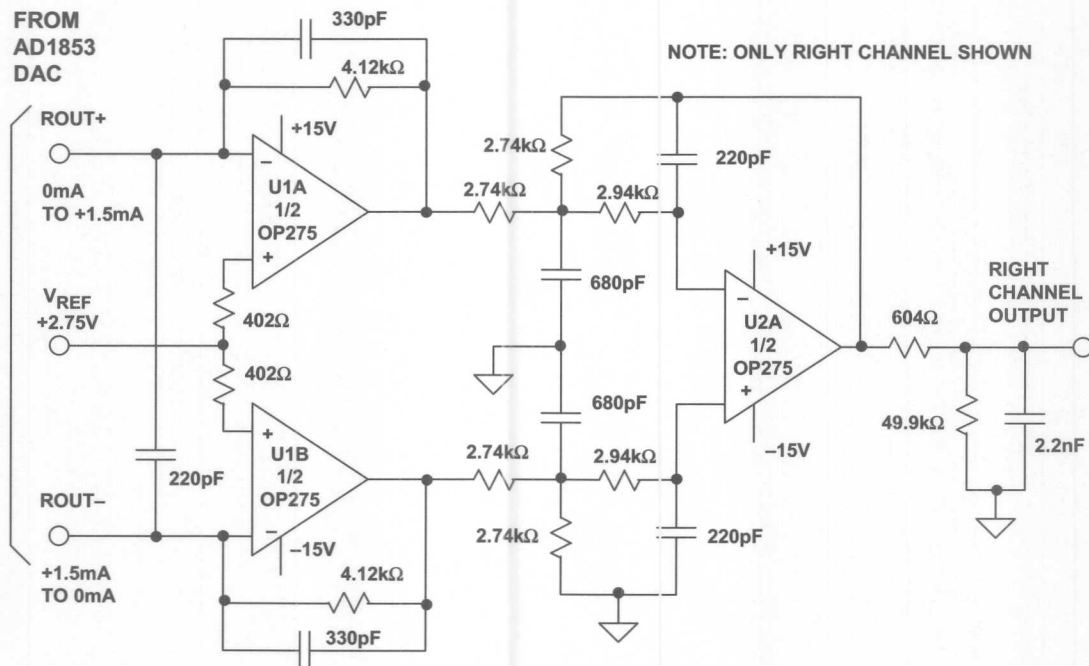
BUFFERING HIGH-SPEED DACs USING AD813X DIFFERENTIAL AMPLIFIER



Op Amp Applications, Chapter 3

2.72

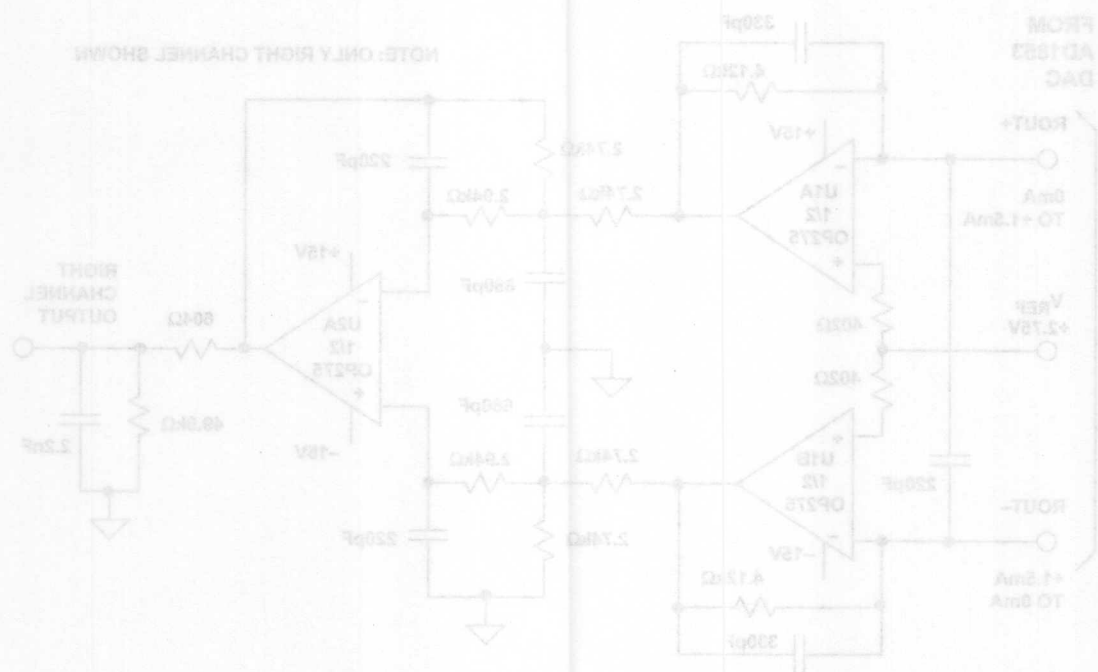
A 75kHz 4-POLE GAUSSIAN ACTIVE FILTER FOR BUFFERING THE OUTPUT OF THE AD1853 STEREO DAC



Op Amp Applications, Chapter 3

2.73

A 75kHz 4-POLE GAUSSIAN ACTIVE FILTER FOR BUFFERING THE OUTPUT OF THE AD1853 STEREO DAC



NOTE: ONLY RIGHT CHANNEL SHOWN

2.73

Op Amp Applications, Chapter 3

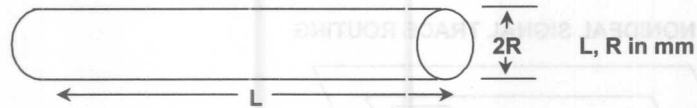
OP AMP APPLICATIONS SEMINAR

1. History, Basics, Design Aids, Filters
2. Specialty Amplifiers, Using Op Amps with Data Converters
3. **Hardware and Housekeeping Design Techniques**
4. Signal Amplifiers, Sensor Signal Conditioning

OP AMP APPLICATIONS SEMINAR

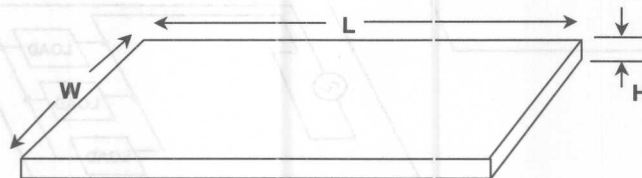
1. History, Basics, Design Aids, Filters
2. Specialty Amplifiers, Using Op Amps with Data Converters
3. Hardware and Housekeeping Design Techniques
4. Signal Amplifiers, Sensor Signal Conditioning

WIRE AND STRIP INDUCTANCE CALCULATIONS



$$\text{WIRE INDUCTANCE} = 0.0002L \left[\ln \left(\frac{2L}{R} \right) - 0.75 \right] \mu\text{H}$$

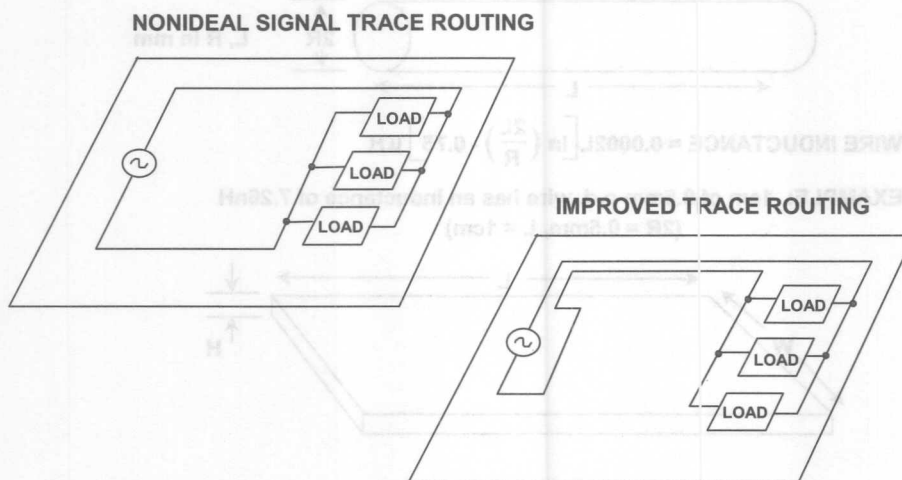
EXAMPLE: 1cm of 0.5mm o.d. wire has an inductance of 7.26nH
($2R = 0.5\text{mm}$, $L = 1\text{cm}$)



$$\text{STRIP INDUCTANCE} = 0.0002L \left[\ln \left(\frac{2L}{W+H} \right) + 0.2235 \left(\frac{W+H}{L} \right) + 0.5 \right] \mu\text{H}$$

EXAMPLE: 1cm of 0.25 mm PC track has an inductance of 9.59 nH
($H = 0.038\text{mm}$, $W = 0.25\text{mm}$, $L = 1\text{cm}$)

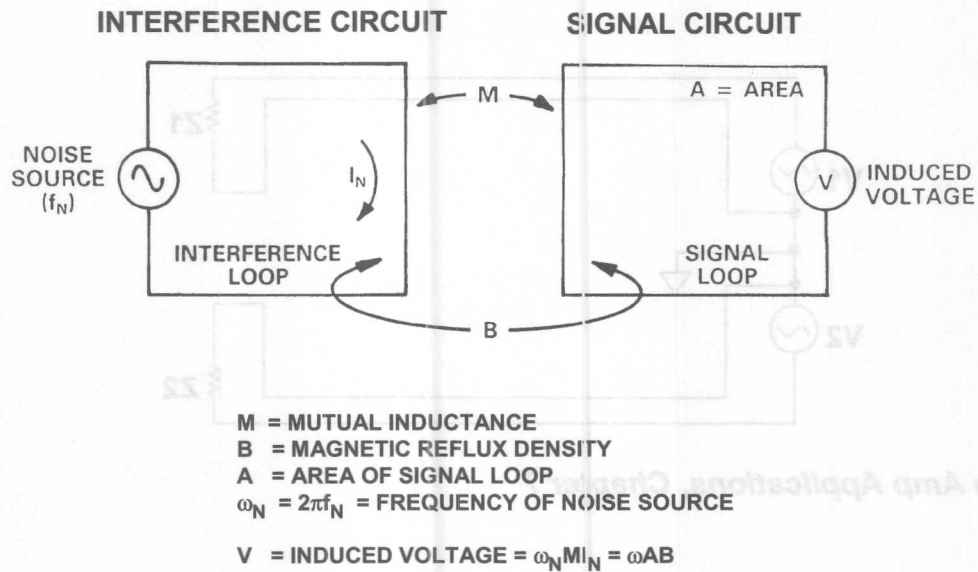
NONIDEAL AND IMPROVED SIGNAL TRACE ROUTING



Op Amp Applications, Chapter 7

3.2

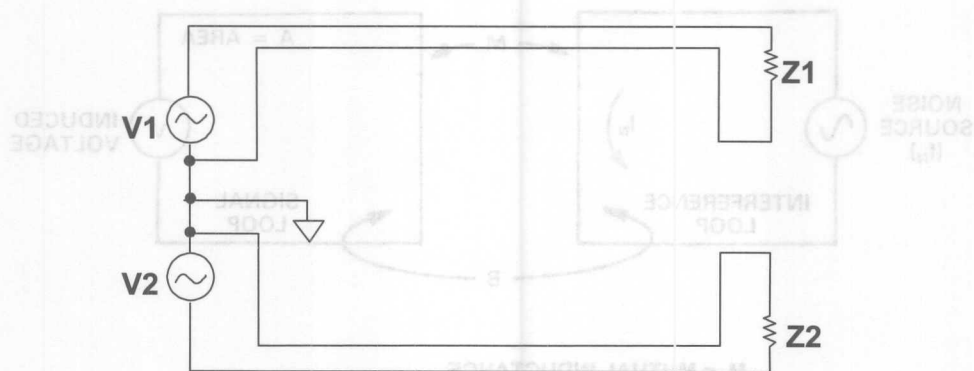
BASIC PRINCIPLES OF INDUCTIVE COUPLING



Op Amp Applications, Chapter 7

3.3

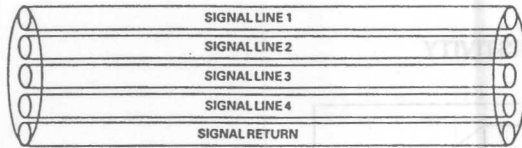
PROPER SIGNAL ROUTING AND LAYOUT CAN REDUCE INDUCTIVE COUPLING



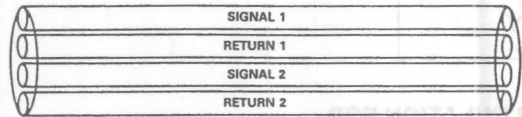
Op Amp Applications, Chapter 7

3.4

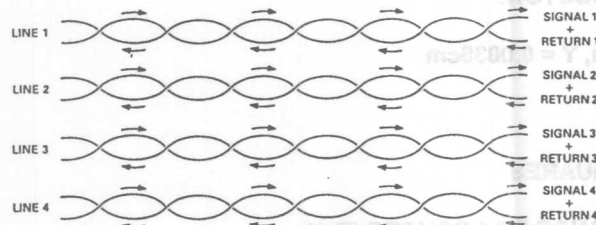
MUTUAL INDUCTANCE AND COUPLING WITHIN SIGNAL CABLING



◆ FLAT RIBBON CABLE WITH SINGLE RETURN HAS LARGE MUTUAL INDUCTANCE BETWEEN CIRCUITS



◆ SEPARATE AND ALTERNATE SIGNAL / RETURN LINES FOR EACH CIRCUIT REDUCES MUTUAL INDUCTANCE



◆ TWISTED PAIRS REDUCE MUTUAL INDUCTANCE STILL FURTHER

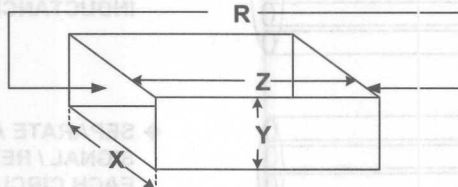
Op Amp Applications, Chapter 7

3.5

CALCULATION OF SHEET RESISTANCE AND LINEAR RESISTANCE FOR STANDARD COPPER PCB CONDUCTORS

$$R = \frac{\rho Z}{XY}$$

ρ = RESISTIVITY



**SHEET RESISTANCE CALCULATION FOR
1 OZ. COPPER CONDUCTOR:**

$$\rho = 1.724 \times 10^{-6} \Omega\text{cm}, Y = 0.0036\text{cm}$$

$$R = 0.48 \frac{Z}{X} \text{ m}\Omega$$

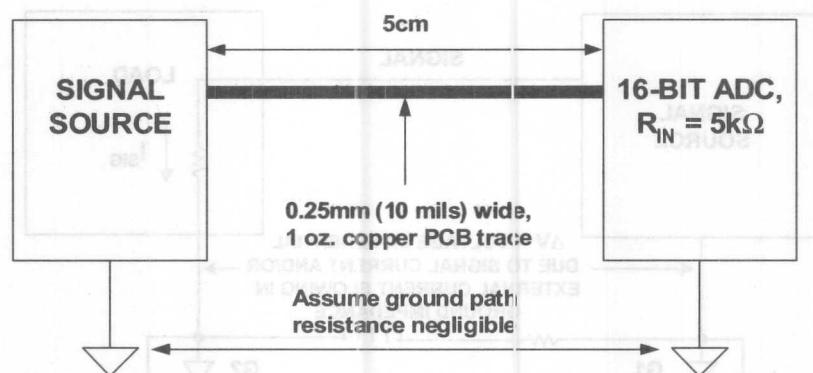
$$\frac{Z}{X} = \text{NUMBER OF SQUARES}$$

$$R = \text{SHEET RESISTANCE OF 1 SQUARE (Z=X)} \\ = 0.48\text{m}\Omega/\text{SQUARE}$$

Op Amp Applications, Chapter 7

3.6

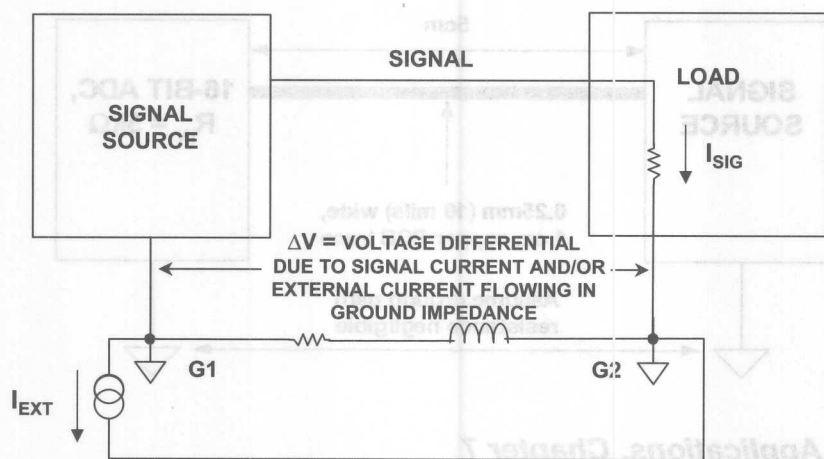
OHM'S LAW PREDICTS >1LSB OF ERROR DUE TO DROP IN PCB CONDUCTOR



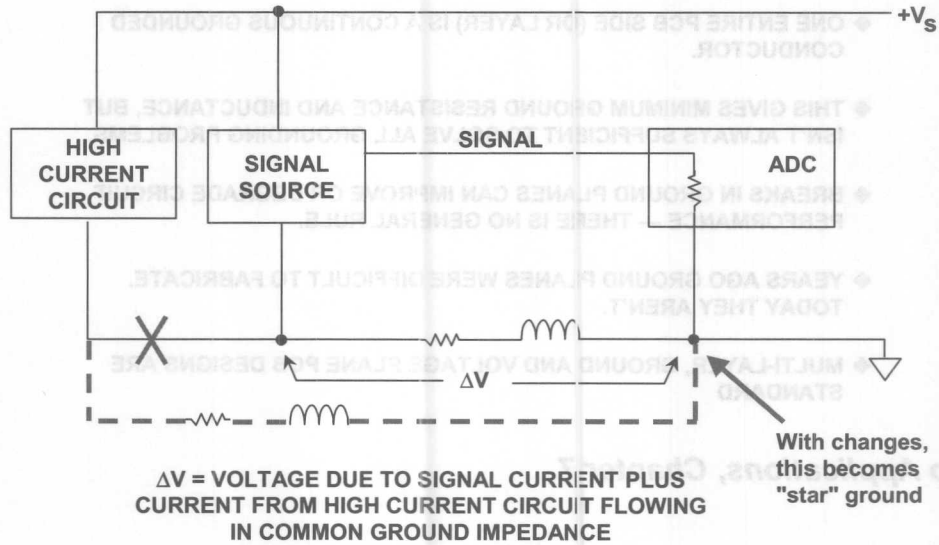
Op Amp Applications, Chapter 7

3.7

A MORE REALISTIC SOURCE-TO-LOAD GROUNDING SYSTEM VIEW INCLUDES CONSIDERATION OF THE IMPEDANCE BETWEEN G1-G2, PLUS THE EFFECT OF ANY NON-SIGNAL-RELATED CURRENTS



ANY CURRENT FLOWING THROUGH A COMMON GROUND IMPEDANCE CAN CAUSE ERRORS



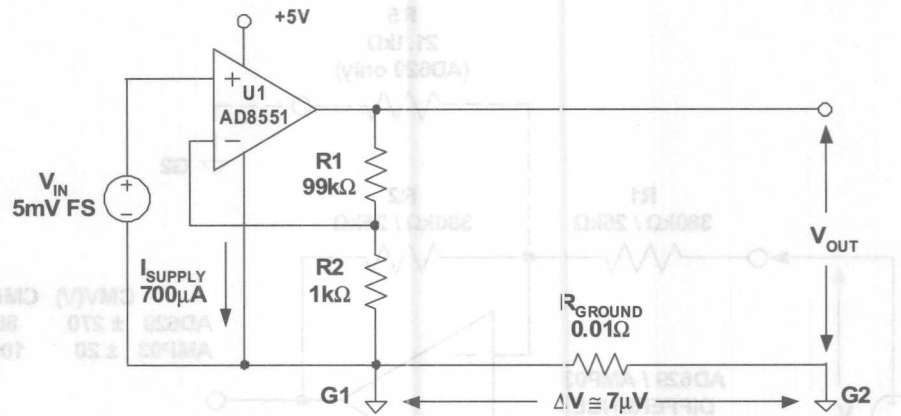
CHARACTERISTICS OF GROUND PLANES

- ◆ ONE ENTIRE PCB SIDE (OR LAYER) IS A CONTINUOUS GROUNDED CONDUCTOR.
- ◆ THIS GIVES MINIMUM GROUND RESISTANCE AND INDUCTANCE, BUT ISN'T ALWAYS SUFFICIENT TO SOLVE ALL GROUNDING PROBLEMS.
- ◆ BREAKS IN GROUND PLANES CAN IMPROVE OR DEGRADE CIRCUIT PERFORMANCE — THERE IS NO GENERAL RULE.
- ◆ YEARS AGO GROUND PLANES WERE DIFFICULT TO FABRICATE. TODAY THEY AREN'T.
- ◆ MULTI-LAYER, GROUND AND VOLTAGE PLANE PCB DESIGNS ARE STANDARD

Op Amp Applications, Chapter 7

3.10

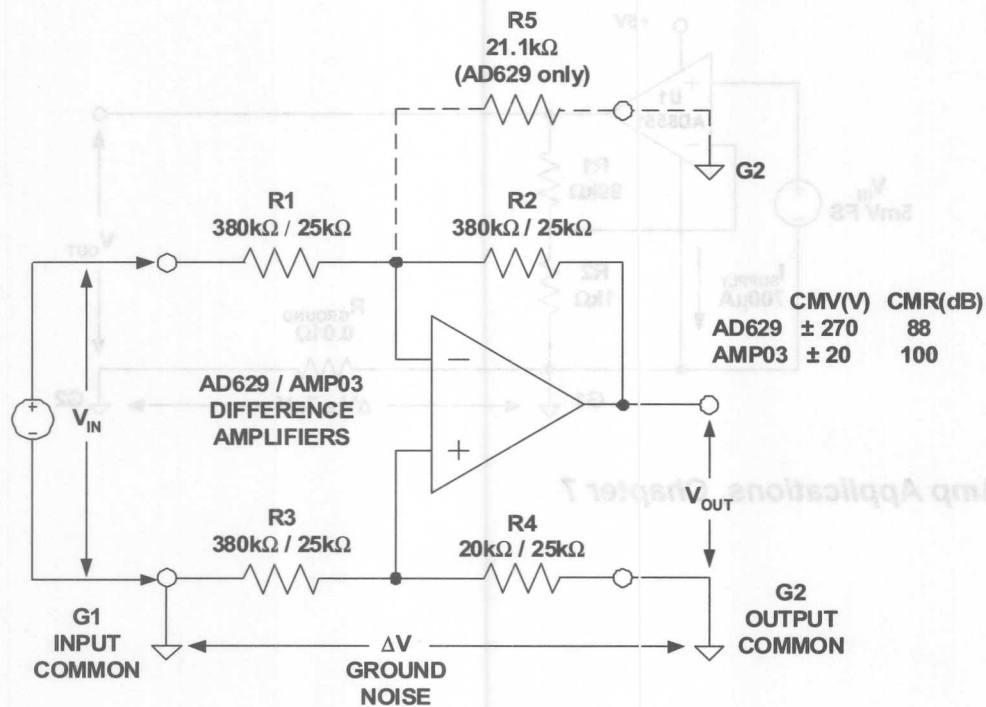
UNLESS CARE IS TAKEN, EVEN SMALL COMMON GROUND CURRENTS CAN DEGRADE PRECISION AMPLIFIER ACCURACY



Op Amp Applications, Chapter 7

3.11

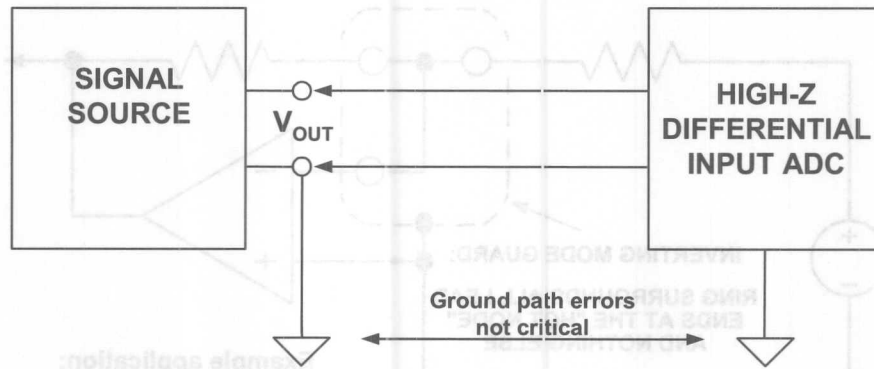
A DIFFERENTIAL INPUT GROUND ISOLATING AMPLIFIER ALLOWS
HIGH TRANSMISSION ACCURACY BY REJECTING GROUND NOISE VOLTAGE BETWEEN
SOURCE (G1) AND MEASUREMENT (G2) GROUNDS



Op Amp Applications, Chapter 7

3.12

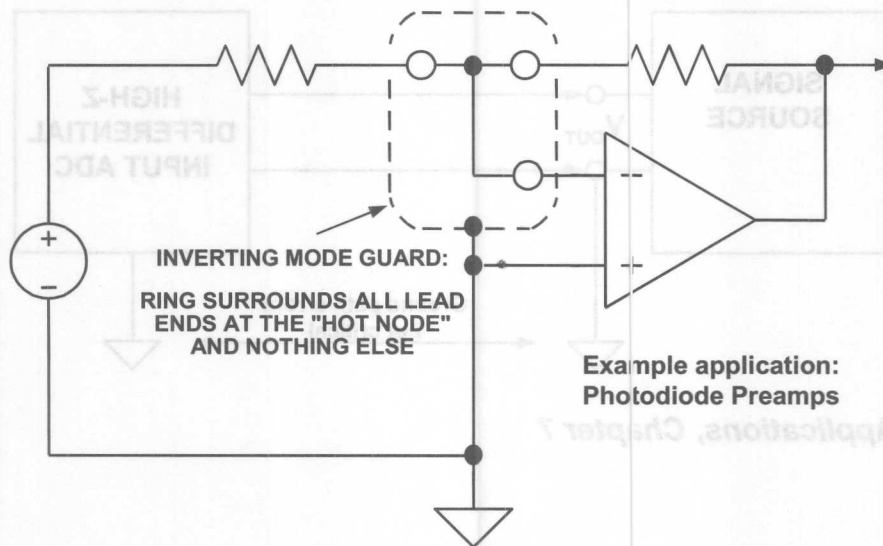
**A HIGH-IMPEDANCE DIFFERENTIAL INPUT ADC ALSO ALLOWS
HIGH TRANSMISSION ACCURACY BETWEEN SOURCE AND LOAD**



Op Amp Applications, Chapter 7

3.13

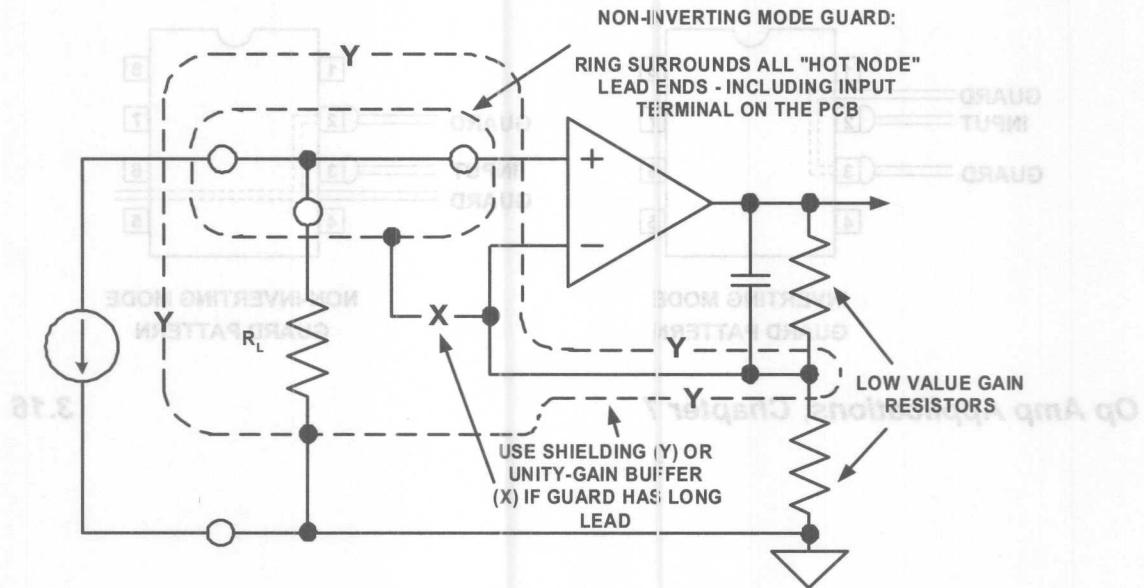
**INVERTING MODE GUARD ENCLOSES ALL OP AMP INVERTING
INPUT CONNECTIONS WITHIN A GROUNDING GUARD RING**



Op Amp Applications, Chapter 7

3.14

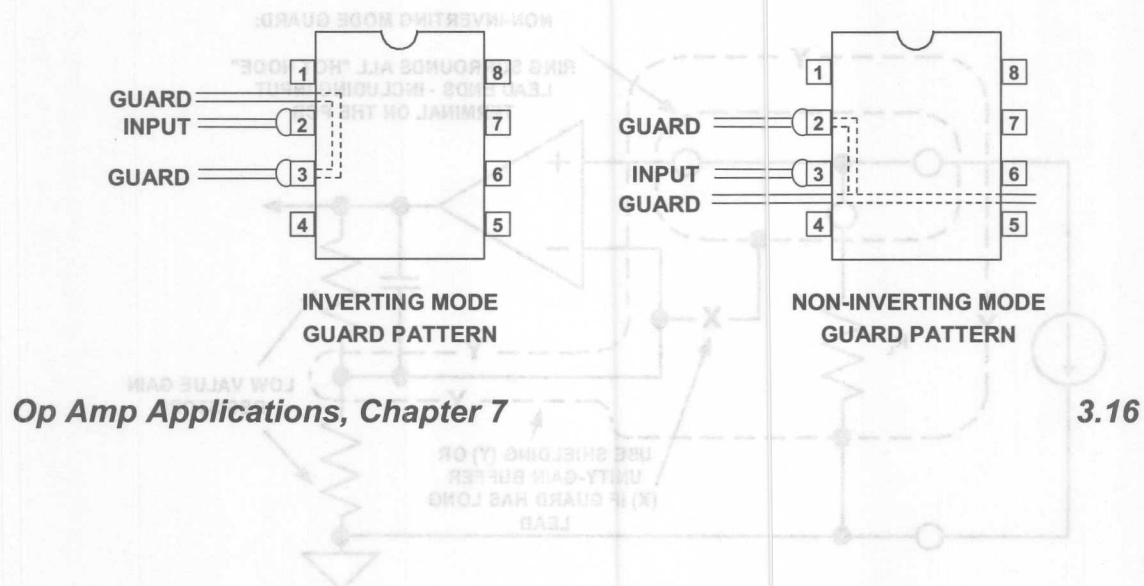
NON-INVERTING MODE GUARD ENCLOSES ALL OP AMP NON-INVERTING INPUT CONNECTIONS WITHIN A LOW IMPEDANCE, DRIVEN GUARD RING



Op Amp Applications, Chapter 7

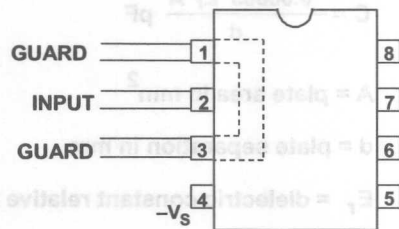
3.15

PCB GUARD PATTERNS FOR INVERTING AND NON-INVERTING MODE OP AMPS USING 8 PIN MINIDIP (N) PACKAGE

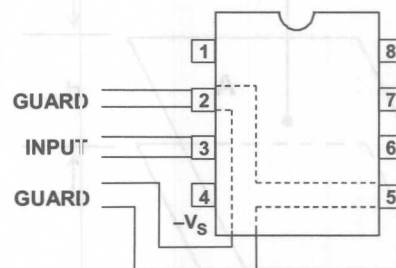


PCB GUARD PATTERNS FOR INVERTING AND NON-INVERTING MODE OP AMPS USING 8 PIN SOIC (R) PACKAGE

NOTE: PINS 1, 5, & 8 ARE OPEN ON MANY "R" PACKAGED DEVICES



INVERTING MODE
GUARD PATTERN

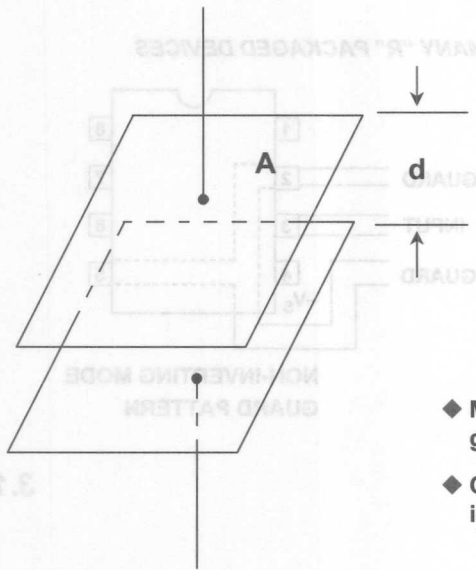


NON-INVERTING MODE
GUARD PATTERN

Op Amp Applications, Chapter 7

3.17

CAPACITANCE OF TWO PARALLEL PLATES



$$C = \frac{0.00885 E_r A}{d} \text{ pF}$$

A = plate area in mm²

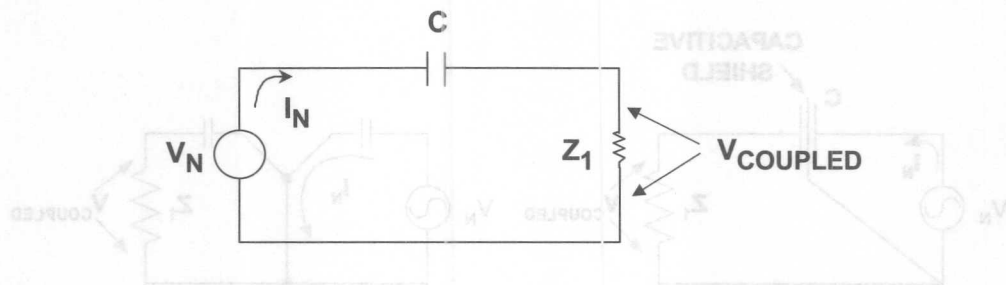
d = plate separation in mm

E_r = dielectric constant relative to air

◆ Most common PCB type uses 1.5mm glass-fiber epoxy material with E_r = 4.7

◆ Capacity of PC track over ground plane is roughly 2.8pF/crn²

CAPACITIVE COUPLING EQUIVALENT CIRCUIT MODEL



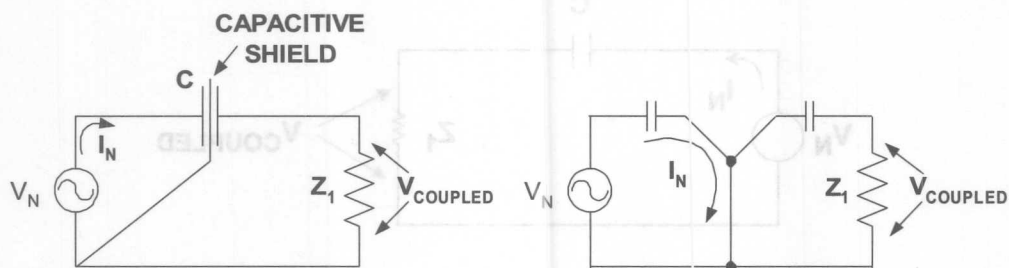
$Z_1 = \text{CIRCUIT IMPEDANCE}$
 $Z_2 = 1/j\omega C$

$$V_{COUPLED} = V_N \left(\frac{Z_1}{Z_1 + Z_2} \right)$$

Op Amp Applications, Chapter 7

3.19

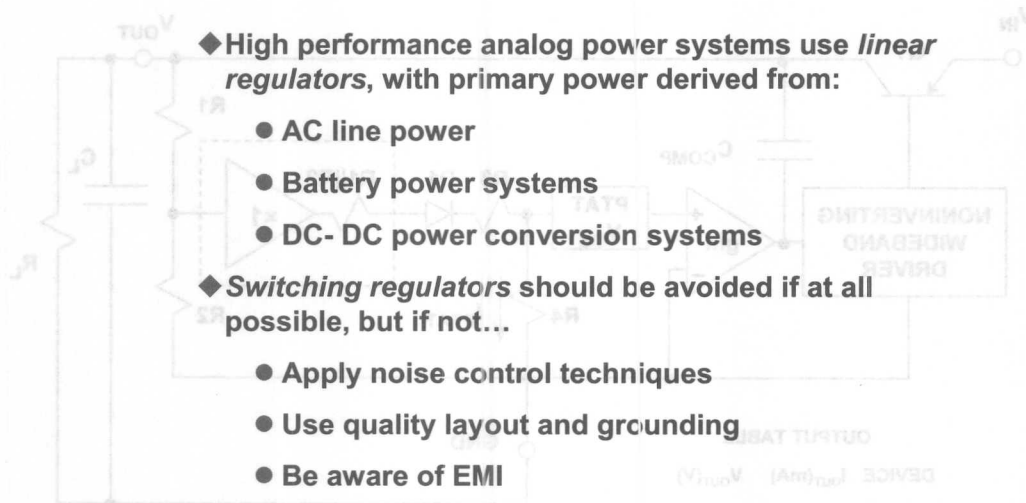
AN OPERATIONAL MODEL OF A FARADAY SHIELD



Op Amp Applications, Chapter 7

3.20

REGULATION PRIORITIES FOR OP AMP POWER SUPPLY SYSTEMS

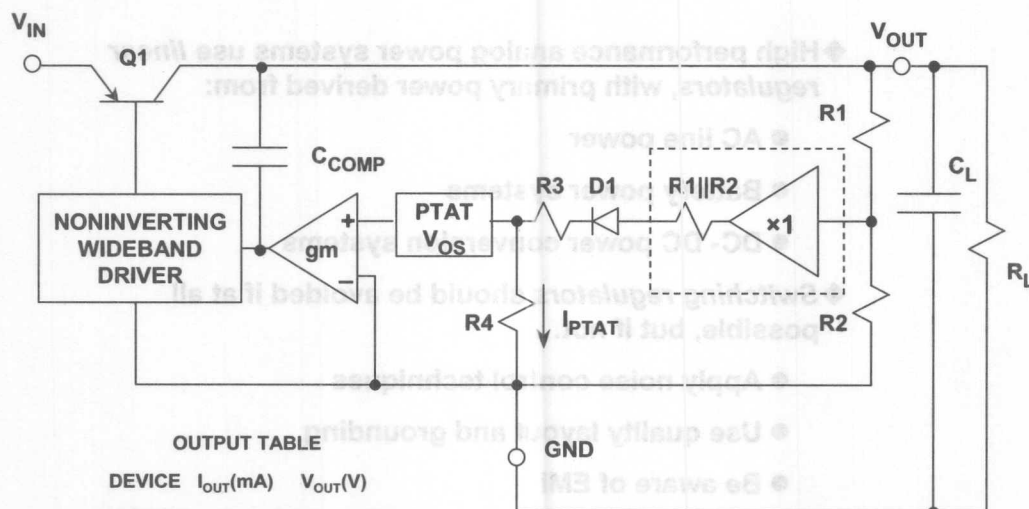


Op Amp Applications, Chapter 7

3.21

DEVICE	I_{OUT} (mA)	V_{OUT} (V)
ADP3306	50	2.7, 3.3, 3.3, 3.3
ADP3301	100	2.7, 3.3, 3.3, 3.3
ADP3302	200	2.7, 3.3, 3.3, 3.3
ADP3328	500	1.8, 2.2, 2.8, 3.3

THE ADP330X anyCAP™ LDO ARCHITECTURE HAS BOTH DC AND AC PERFORMANCE ADVANTAGES



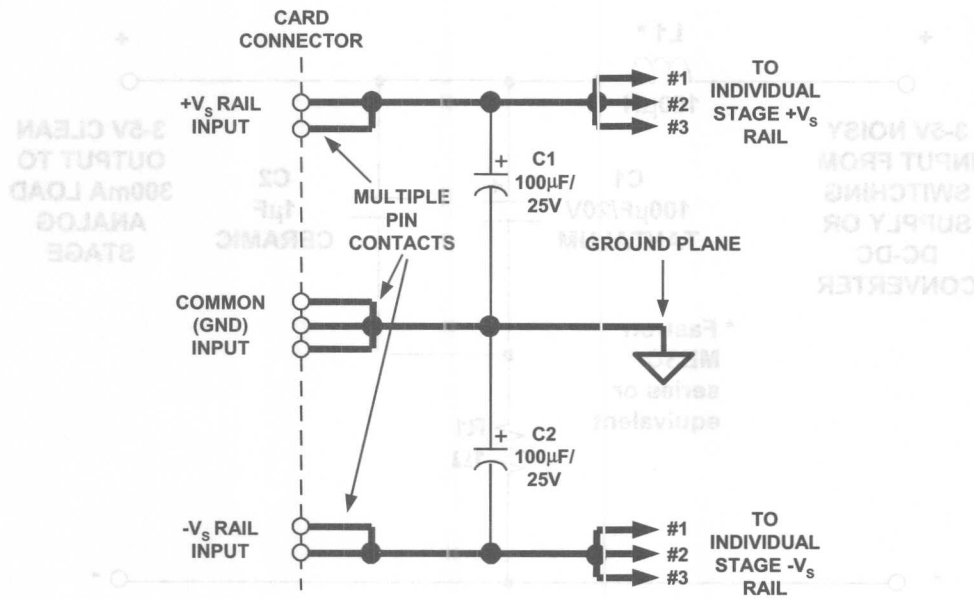
OUTPUT TABLE

DEVICE	$I_{OUT}(mA)$	$V_{OUT}(V)$
ADP3300	50	2.7, 3, 3.2, 3.3, 5
ADP3301	100	2.7, 3, 3.2, 3.3, 5
ADP3303	200	2.7, 3, 3.2, 3.3, 5
ADP3335	500	1.8, 2.5, 2.85, 3.3, 5

Op Amp Applications, Chapter 7

3.22

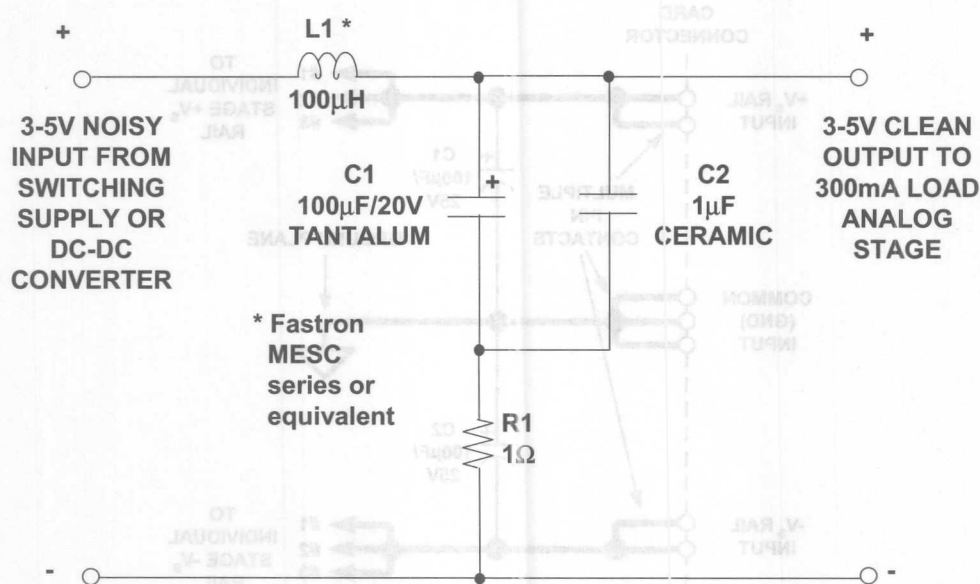
DUAL-SUPPLY LOW FREQUENCY RAIL BYPASS/DISTRIBUTION FILTER



Op Amp Applications, Chapter 7

3.23

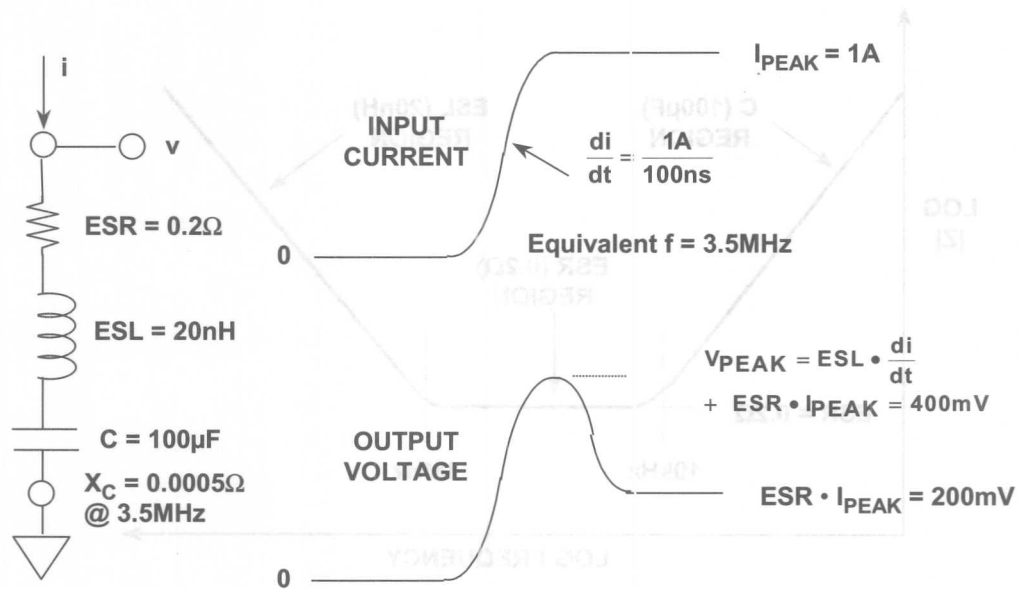
A CARD-ENTRY FILTER IS USEFUL FOR LOW-MEDIUM FREQUENCY POWER LINE NOISE FILTERING IN ANALOG SYSTEMS



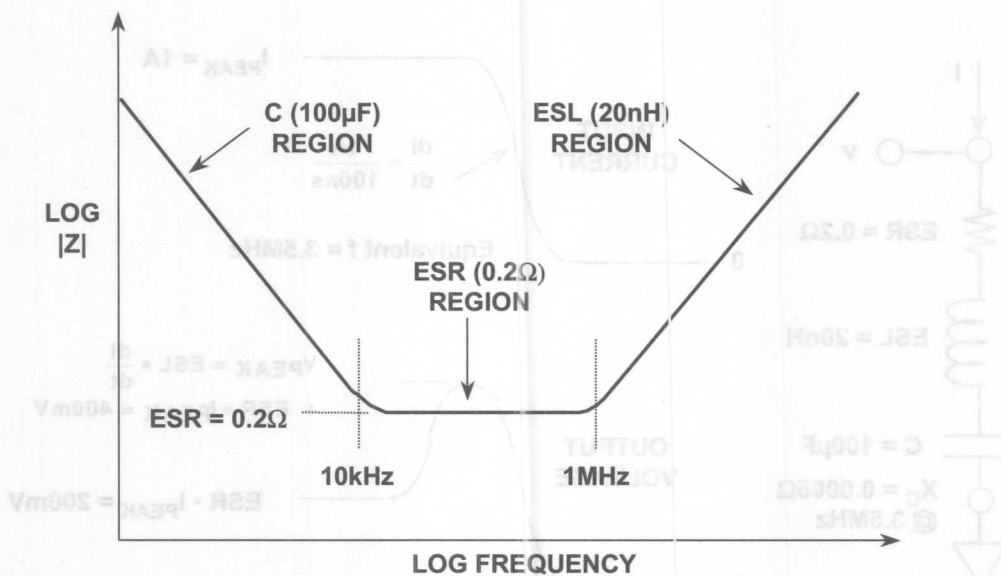
Op Amp Applications, Chapter 7

3.24

CAPACITOR EQUIVALENT CIRCUIT AND RESPONSE TO INPUT CURRENT PULSE



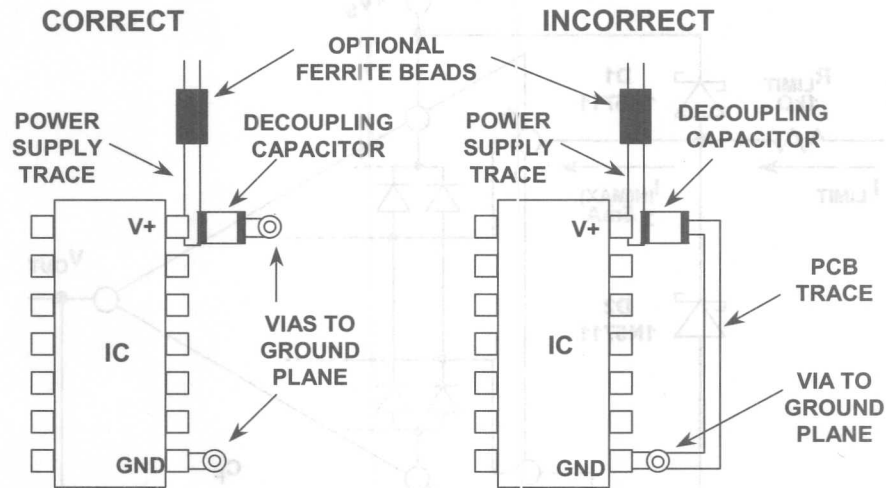
ELECTROLYTIC CAPACITOR IMPEDANCE VERSUS FREQUENCY



Op Amp Applications, Chapter 7

3.26

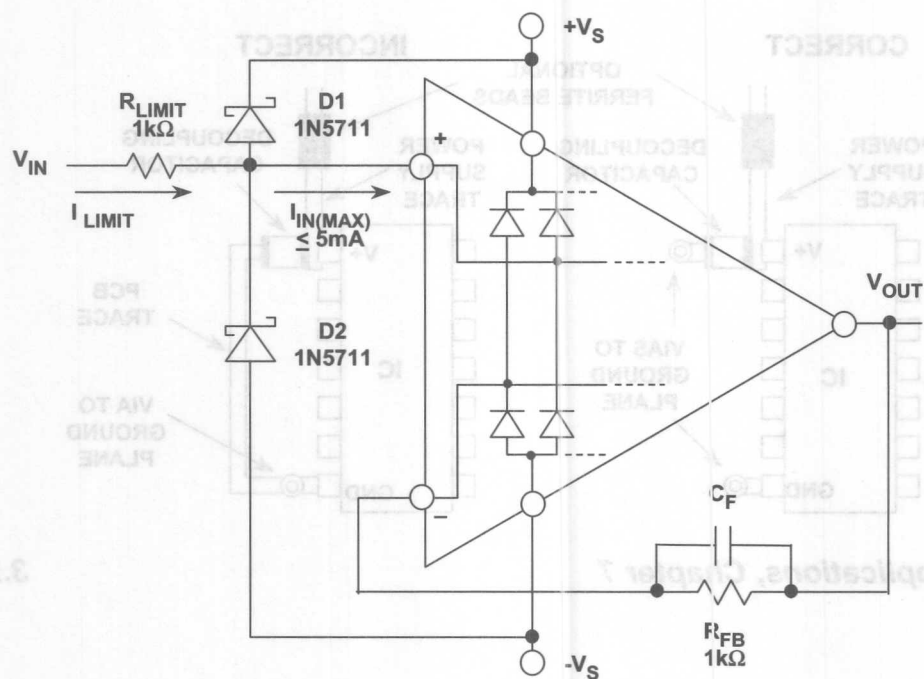
LOCALIZED HIGH FREQUENCY SUPPLY FILTER(S) PROVIDES OPTIMUM FILTERING AND DECOUPLING VIA SHORT LOW-INDUCTANCE PATH (GROUND PLANE)



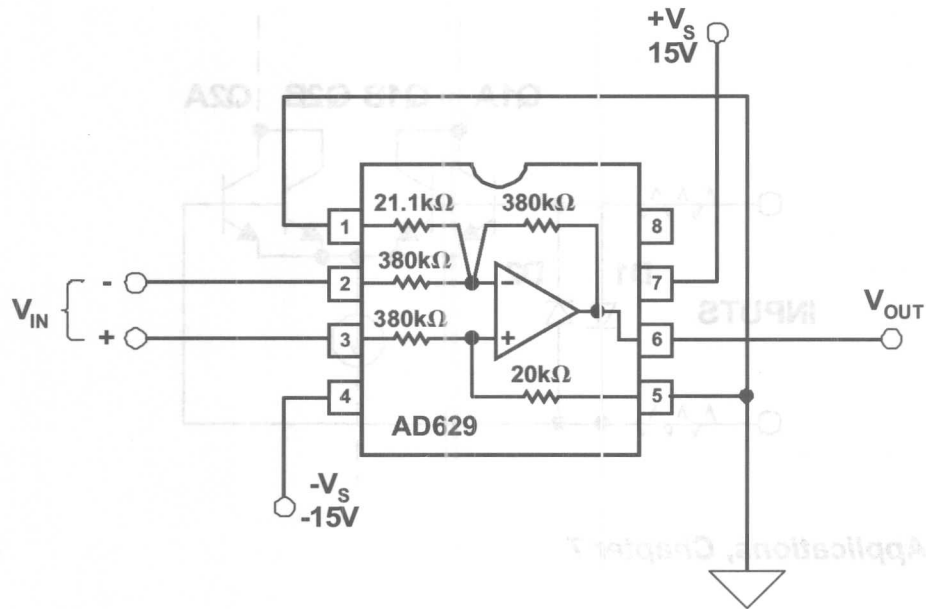
Op Amp Applications, Chapter 7

3.27

A GENERAL-PURPOSE OP AMP CM OVER-VOLTAGE PROTECTION NETWORK USING SCHOTTKY CLAMP DIODES WITH CURRENT LIMIT RESISTANCE



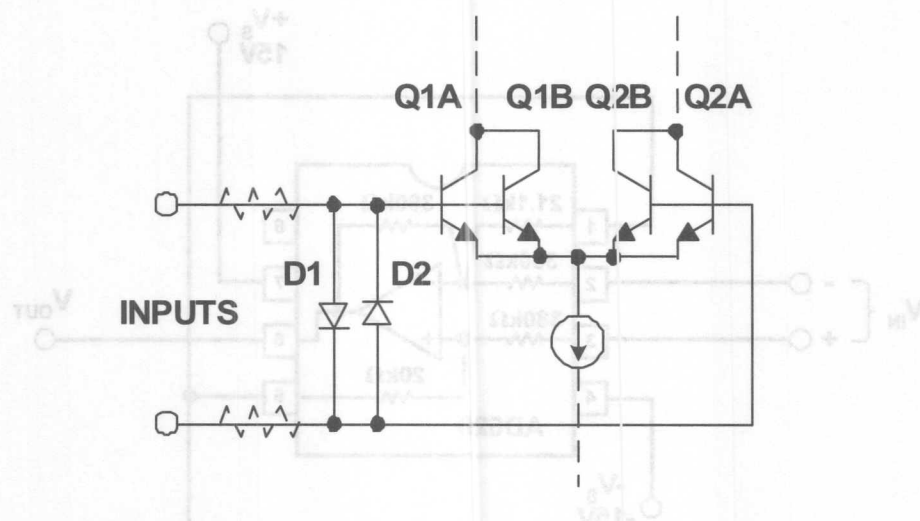
THE AD629 HIGH VOLTAGE IN-AMP IC OFFERS $\pm 500\text{V}$ INPUT OVER-VOLTAGE PROTECTION, ONE-COMPONENT SIMPLICITY, AND FAIL-SAFE POWER OFF OPERATION



Op Amp Applications, Chapter 7

3.29

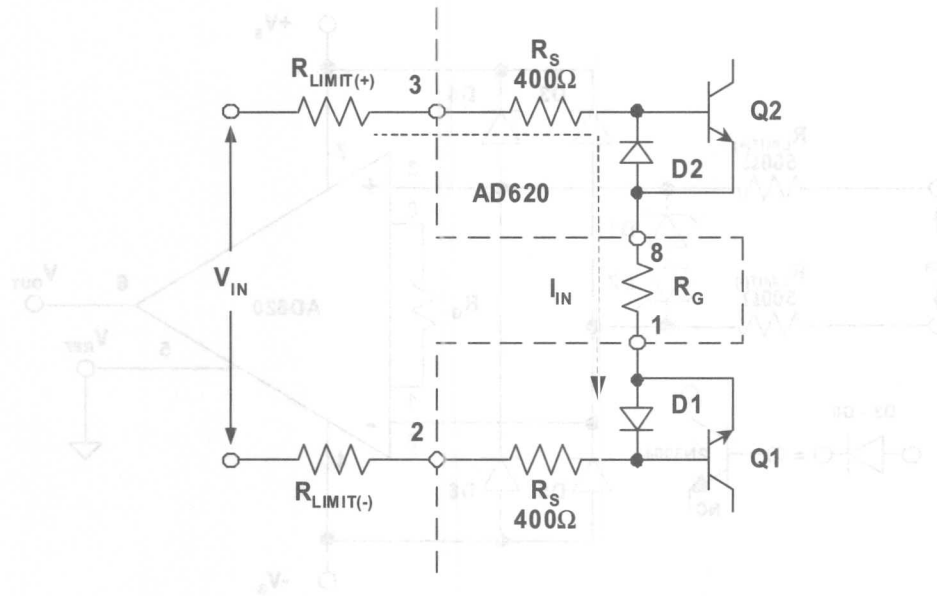
AN OP AMP INPUT STAGE WITH D1-D2 INPUT DIFFERENTIAL OVER-VOLTAGE PROTECTION NETWORK



Op Amp Applications, Chapter 7

3.30

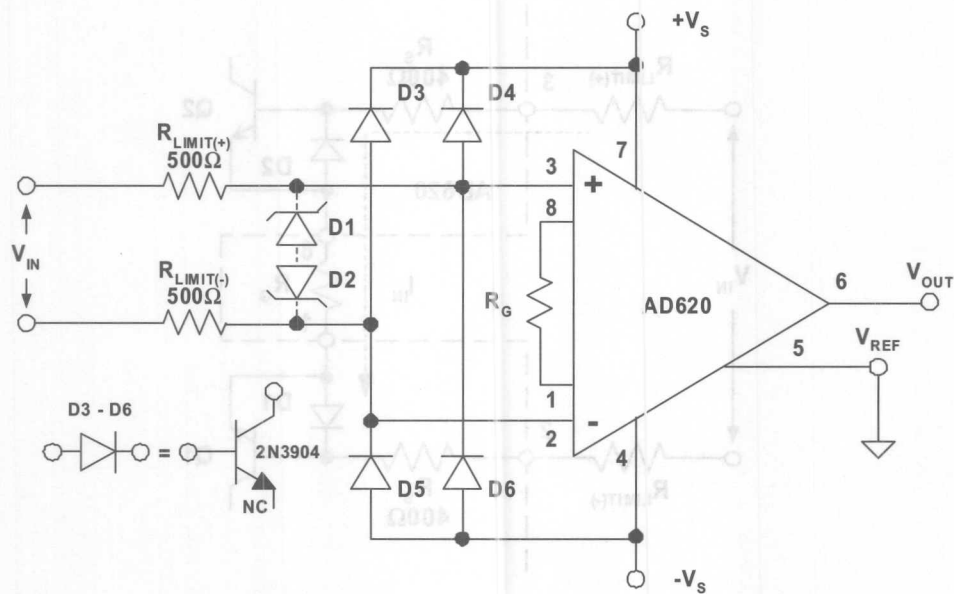
THE AD620 IN-AMP INPUT INTERNALLY USES D1-D2 AND SERIES RESISTORS R_S FOR PROTECTION (ADDITIONAL PROTECTION CAN BE ADDED EXTERNALLY)



Op Amp Applications, Chapter 7

3.31

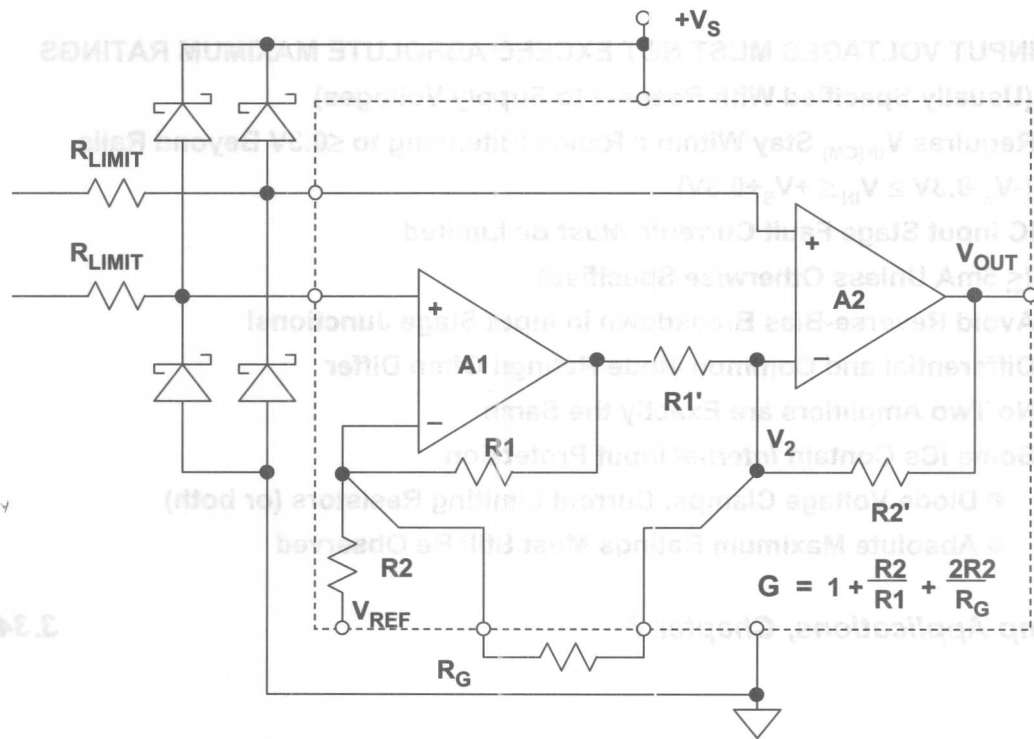
A GENERALIZED DIODE PROTECTION CIRCUIT FOR THE AD620 AND OTHER IN-AMPS
USES D3-D6 FOR CM CLAMPING AND SERIES RESISTORS R_{LIMIT} FOR PROTECTION



Op Amp Applications, Chapter 7

3.32

SINGLE-SUPPLY IN-AMPS MAY OR MAY NOT REQUIRE EXTERNAL PROTECTION IN THE FORM OF RESISTORS AND CLAMP DIODES — IF SO, THEY CAN BE ADDED AS SHOWN



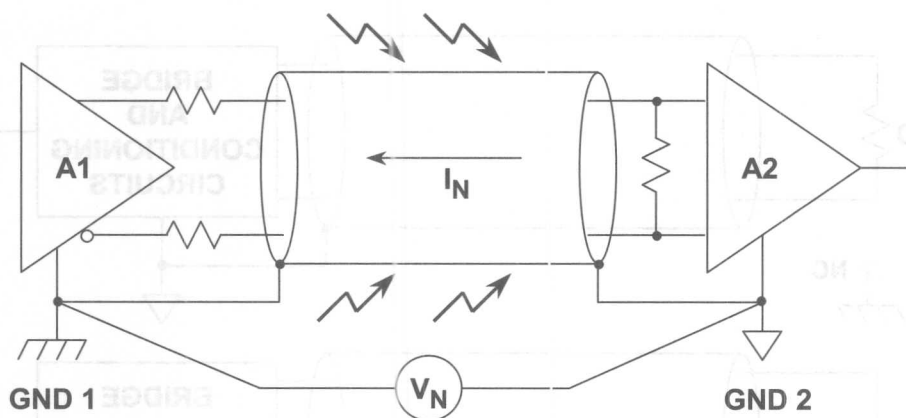
A SUMMARY OF IN-CIRCUIT OVER-VOLTAGE POINTS

- ◆ INPUT VOLTAGES MUST NOT EXCEED ABSOLUTE MAXIMUM RATINGS
(Usually Specified With Respect to Supply Voltages)
- ◆ Requires $V_{IN(CM)}$ Stay Within a Range Extending to $\leq 0.3V$ Beyond Rails
($-V_S - 0.3V \geq V_{IN} \leq +V_S + 0.3V$)
- ◆ IC Input Stage Fault Currents *Must* Be Limited
($\leq 5mA$ Unless Otherwise Specified)
- ◆ Avoid Reverse-Bias Breakdown in Input Stage Junctions!
- ◆ Differential and Common Mode Ratings Often Differ
- ◆ No Two Amplifiers are Exactly the Same
- ◆ Some ICs Contain *Internal* Input Protection
 - Diode Voltage Clamps, Current Limiting Resistors (or both)
 - Absolute Maximum Ratings Must Still Be Observed

Op Amp Applications, Chapter 7

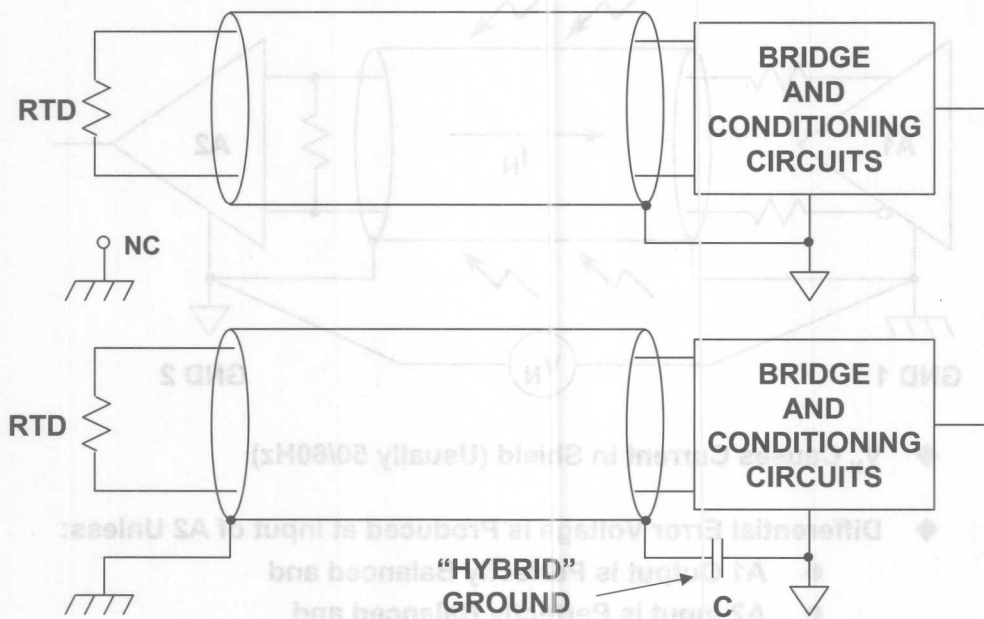
3.34

GROUND LOOPS IN SHIELDED TWISTED PAIR CABLE CAN CAUSE ERRORS



- ◆ V_N Causes Current in Shield (Usually 50/60Hz)
- ◆ Differential Error Voltage is Produced at Input of A2 Unless:
 - A1 Output is Perfectly Balanced and
 - A2 Input is Perfectly Balanced and
 - Cable is Perfectly Balanced

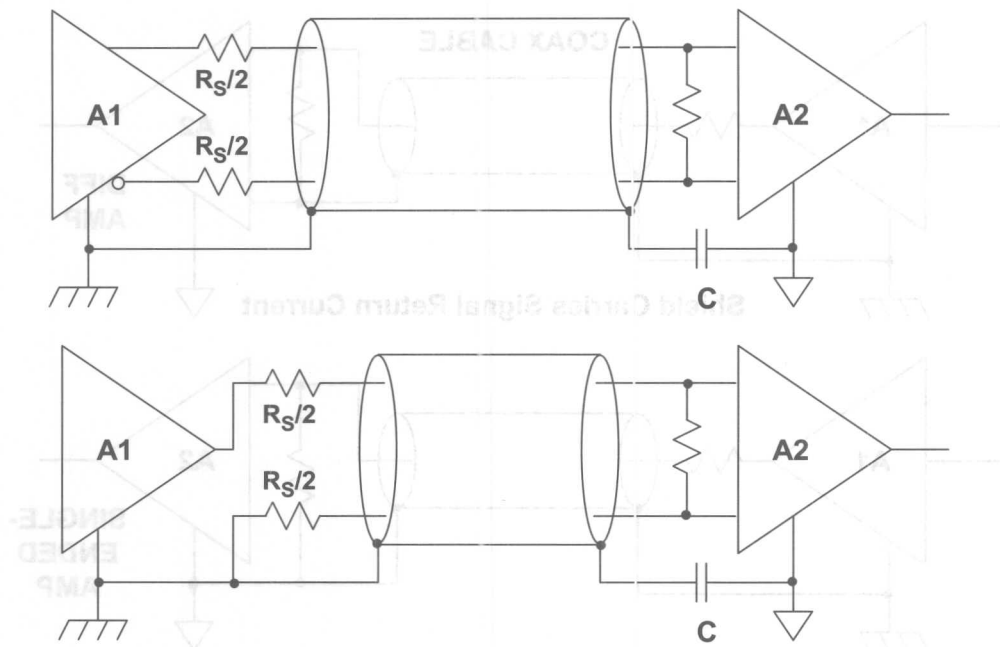
HYBRID GROUNDING OF SHIELDED CABLE WITH PASSIVE SENSOR



Op Amp Applications, Chapter 7

3.36

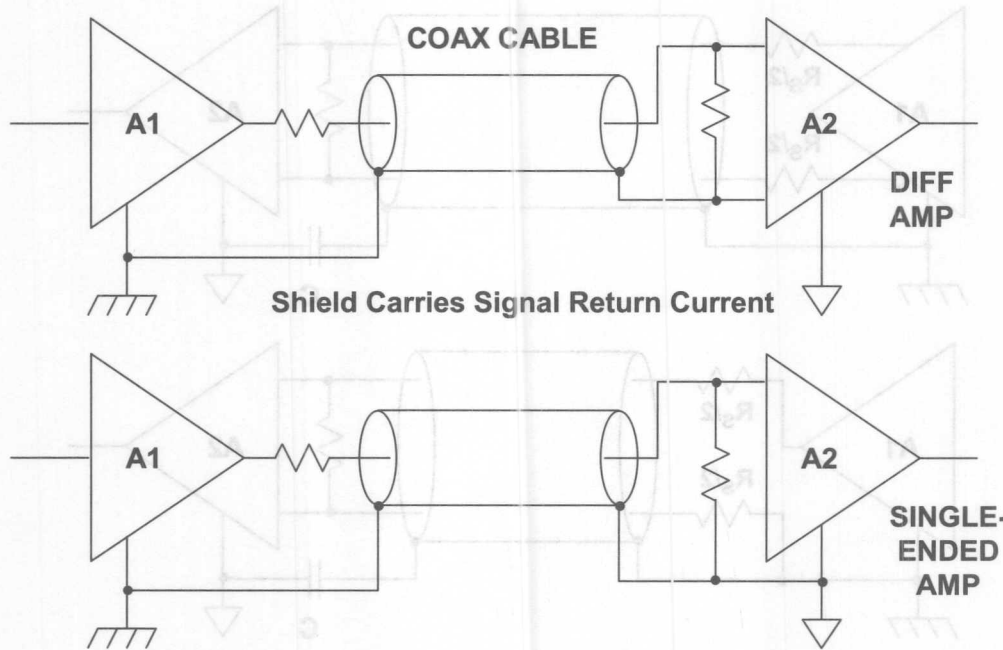
**IMPEDANCE-BALANCED DRIVE OF BALANCED SHIELDED CABLE AIDS NOISE-
IMMUNITY WITH EITHER BALANCED OR SINGLE-ENDED SOURCE SIGNALS**



Op Amp Applications, Chapter 7

Op Amp Applications, Chapter 7 3.37

COAXIAL CABLES CAN USE EITHER BALANCED OR SINGLE-ENDED RECEIVERS



Op Amp Applications, Chapter 7

Op Amp Applications, Chapter 7 3.38

SOME GENERAL OBSERVATIONS ON OP AMP AND IN-AMP INPUT STAGE RFI RECTIFICATION SENSITIVITY

- ◆ BJT input devices *rectify readily*
 - Forward-biased B-E junction
 - Exponential I-V Transfer Characteristic
- ◆ FET input devices *less sensitive to rectifying*
 - Reversed-biased p-n junction
 - Square-law I-V Transfer Characteristic
- ◆ Low I_{supply} devices versus High I_{supply} devices
 - Low $I_{\text{supply}} \Rightarrow$ *Higher rectification sensitivity*
 - High $I_{\text{supply}} \Rightarrow$ *Lower rectification sensitivity*

Op Amp Applications, Chapter 7

3.39

RELATIVE SENSITIVITY COMPARISON - BJT VERSUS JFET

◆ BJT:

Emitter area = $576\mu\text{m}^2$

$I_C = 10\mu\text{A}$

$V_T = 25.68\text{mV @ } 25^\circ\text{C}$

$$\begin{aligned}\Delta i_C &= \left(\frac{V_X}{V_T}\right)^2 \cdot \frac{I_C}{4} \\ &= \frac{V_X^2}{264}\end{aligned}$$

◆ JFET:

$I_{DSS} = 20\mu\text{A (Z/L=1)}$

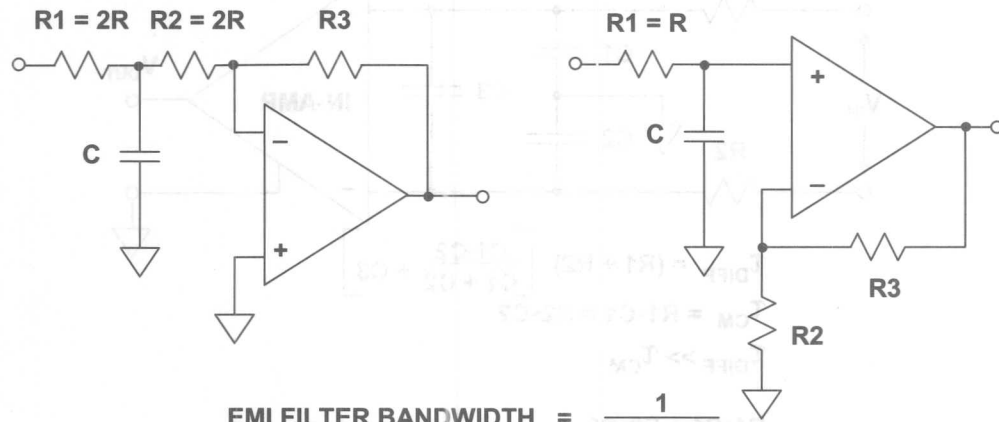
$V_P = 2\text{V}$

$I_D = 10\mu\text{A}$

$$\begin{aligned}\Delta i_D &= \left(\frac{V_X}{V_P}\right)^2 \cdot \frac{I_{DSS}}{2} \\ &= \frac{V_X^2}{400 \times 10^3}\end{aligned}$$

◆ Conclusion: *BJTs ~1500 more sensitive than JFETs!*

SIMPLE EMI/RFI NOISE FILTERS FOR OP AMP CIRCUITS



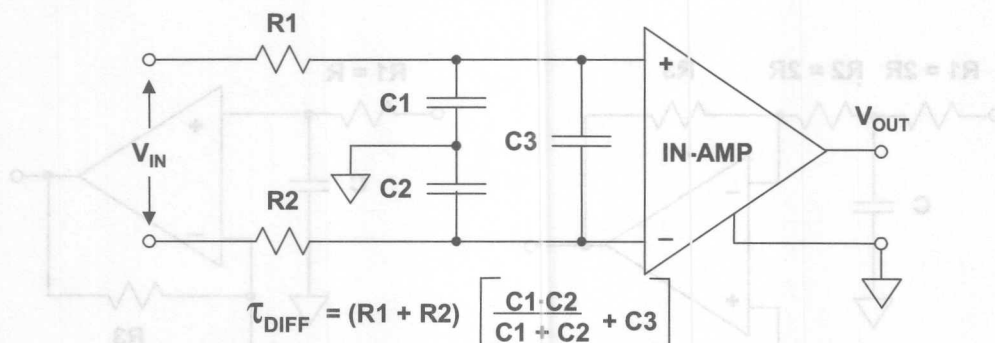
$$\text{EMI FILTER BANDWIDTH} = \frac{1}{2\pi R C}$$

> 100× SIGNAL BANDWIDTH

Op Amp Applications, Chapter 7

3.41

A GENERAL-PURPOSE COMMON-MODE/DIFFERENTIAL-MODE RC EMI/RFI FILTER FOR IN-AMPS



$$\tau_{\text{DIFF}} = (R1 + R2) \left[\frac{C1 \cdot C2}{C1 + C2} + C3 \right]$$

$$\tau_{\text{CM}} = R1 \cdot C1 = R2 \cdot C2$$

$$\tau_{\text{DIFF}} \gg \tau_{\text{CM}}$$

$$R1 \cdot C1 = R2 \cdot C2$$

R1 = R2 SHOULD BE 1% RESISTORS

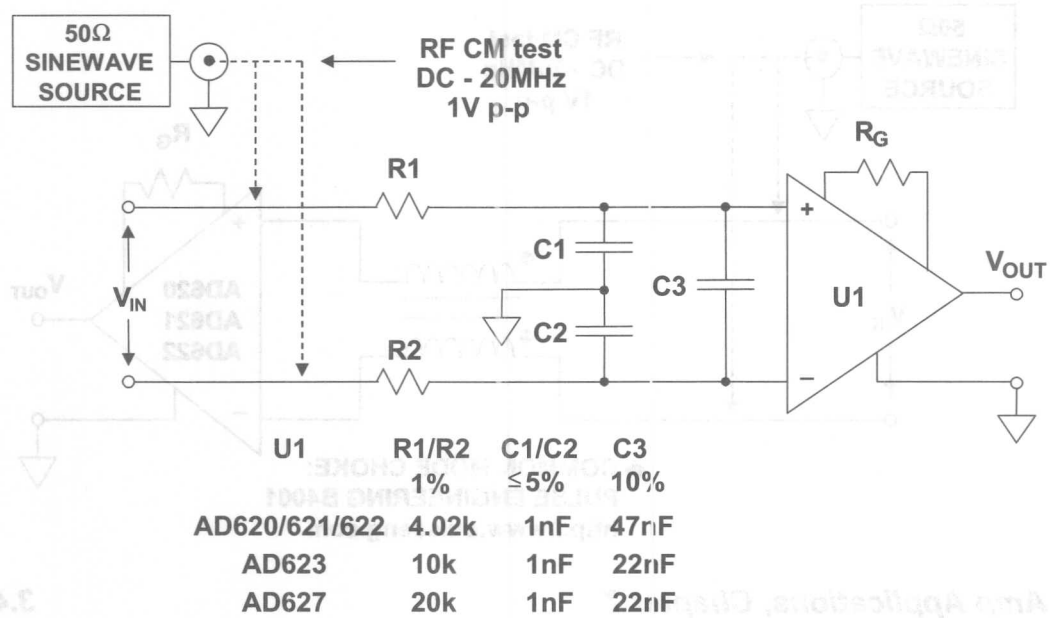
C1 = C2 SHOULD BE ≤ 5% CAPACITORS

$$\text{DIFFERENTIAL FILTER BANDWIDTH} = \frac{1}{2\pi (R1 + R2) \left[\frac{C1 \cdot C2}{C1 + C2} + C3 \right]}$$

Op Amp Applications, Chapter 7

3.42

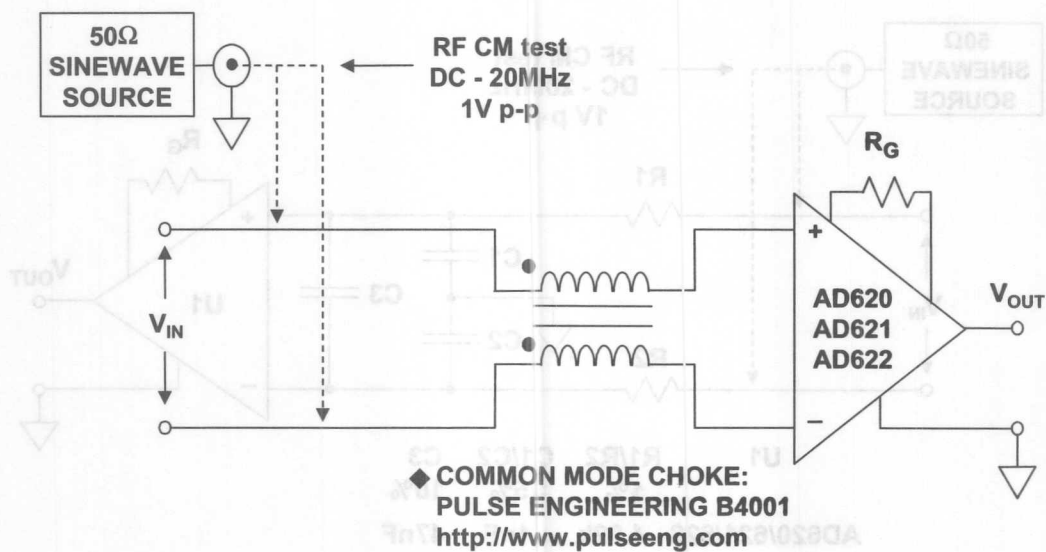
FLEXIBLE COMMON-MODE AND DIFFERENTIAL-MODE RC EMI/RFI FILTERS ARE USEFUL WITH THE AD620 SERIES, THE AD623, AD627, AND OTHER IN-AMPS



Op Amp Applications, Chapter 7

3.43

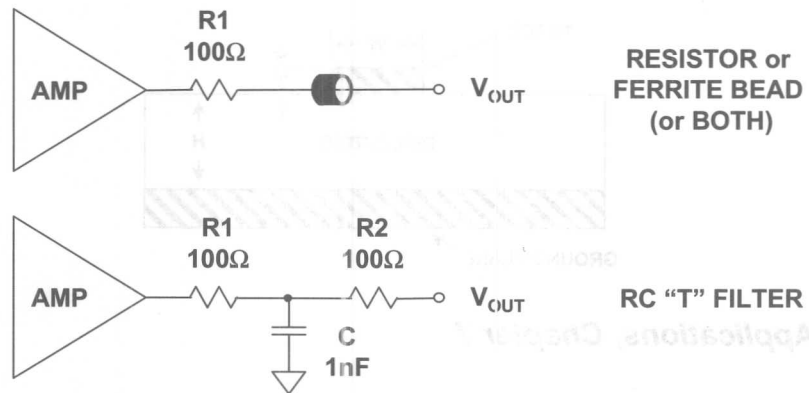
FOR SIMPLICITY AS WELL AS LOWEST NOISE EMI/RFI FILTER OPERATION, A COMMON-MODE CHOKE IS USEFUL WITH THE AD620 SERIES IN-AMP DEVICES



Op Amp Applications, Chapter 7

3.44

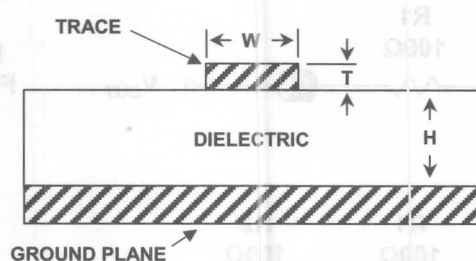
OP AMP AND IN-AMP OUTPUTS SHOULD BE PROTECTED AGAINST EMI/RFI, PARTICULARLY IF THEY DRIVE LONG CABLES



Op Amp Applications, Chapter 7

3.45

A MICROSTRIP TRANSMISSION LINE WITH DEFINED IMPEDANCE IS FORMED BY A PCB TRACE OF APPROPRIATE GEOMETRY, SPACED FROM A GROUND PLANE

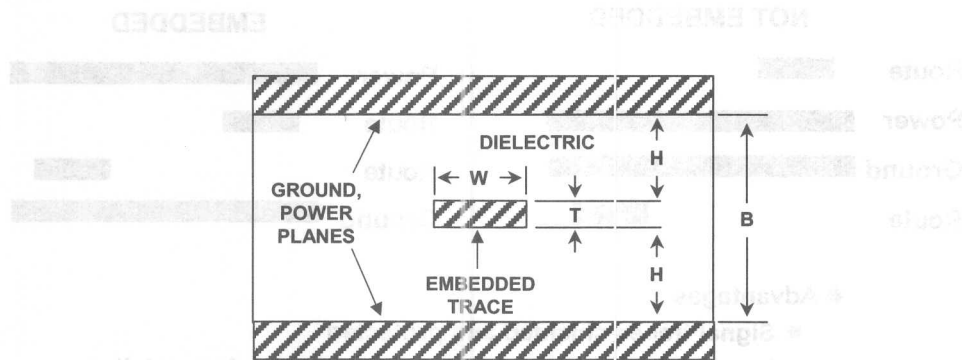


Op Amp Applications, Chapter 7

3.46

HARDWARE AND HOUSEKEEPING DESIGN TECHNIQUES

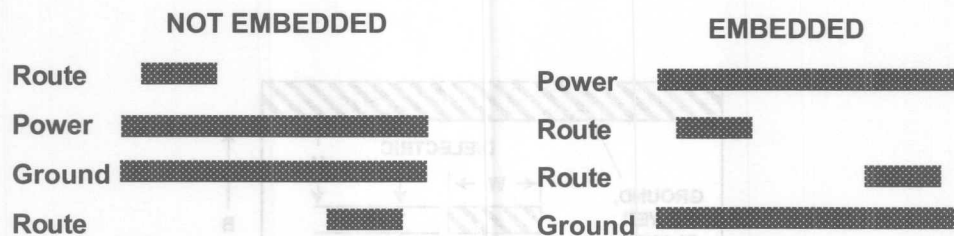
A SYMMETRIC STRIPLINE TRANSMISSION LINE WITH DEFINED IMPEDANCE IS FORMED BY A PCB TRACE OF APPROPRIATE GEOMETRY EMBEDDED BETWEEN EQUALLY SPACED GROUND AND/OR POWER PLANES



Op Amp Applications, Chapter 7

3.47

THE PROS AND CONS OF NOT EMBEDDING VS. THE EMBEDDING OF SIGNAL TRACES IN MULTI-LAYER PCB DESIGNS



◆ Advantages

- Signal traces shielded and protected
- Lower impedance, thus lower emissions and crosstalk
- Significant improvement > 50MHz

◆ Disadvantages

- Difficult prototyping and troubleshooting
- Decoupling may be more difficult
- Impedance may be too low for easy matching

USED WISELY, SIMULATION IS A POWERFUL DESIGN TOOL

- ◆ Understand Realistic Simulation Goals
- ◆ Evaluate Available Models Accordingly
- ◆ Know the Capabilities for Each Competing Op Amp Model
- ◆ Following Simulation, *Breadboarding is Always Desirable and Necessary*
- ◆ Breadboarding / prototyping may require an actual PC board layout

Op Amp Applications, Chapter 7

3.49

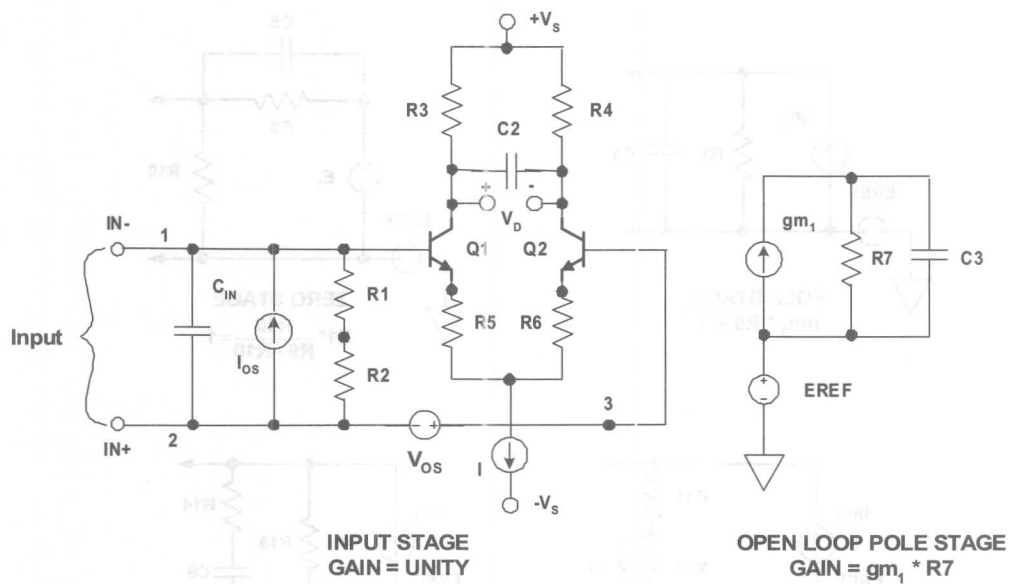
DIFFERENTIATING THE MACROMODEL AND MICROMODEL

	METHODOLOGY	ADVANTAGES	DISADVANTAGES
MACROMODEL	Ideal Elements Model Device Behavior	Fast Simulation Time, Easily Modified	My Not Model All Characteristics
MICROMODEL	Fully Characterized Transistor Level Circuit	Most Complete Model	Slow Simulation Possible, Convergence Difficulty, Non-Availability

Op Amp Applications, Chapter 7

3.50

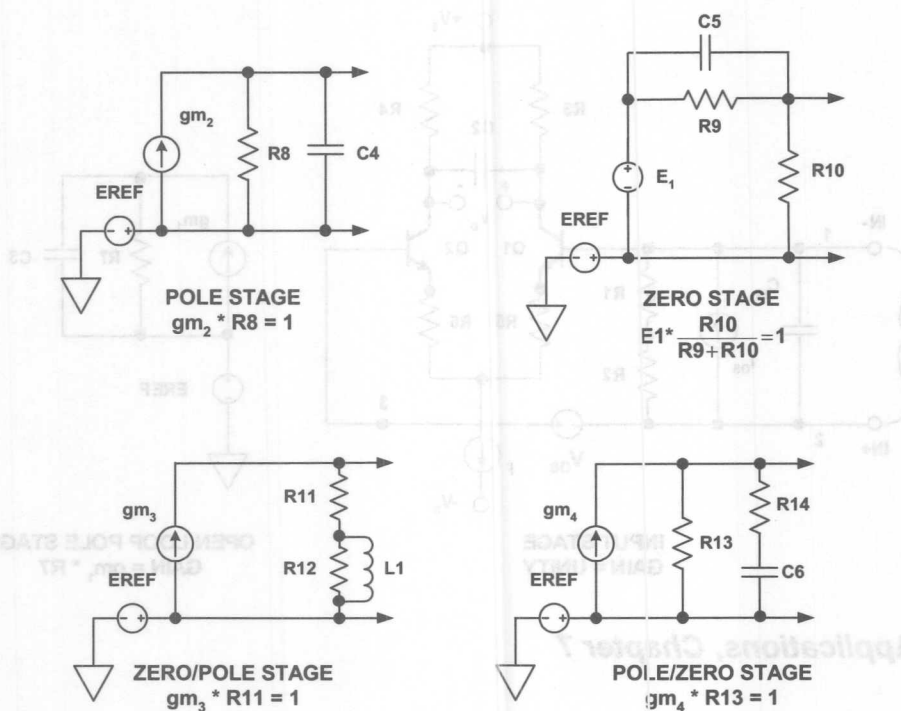
INPUT AND GAIN/POLE STAGES OF ADSpice MACROMODEL



Op Amp Applications, Chapter 7

3.51

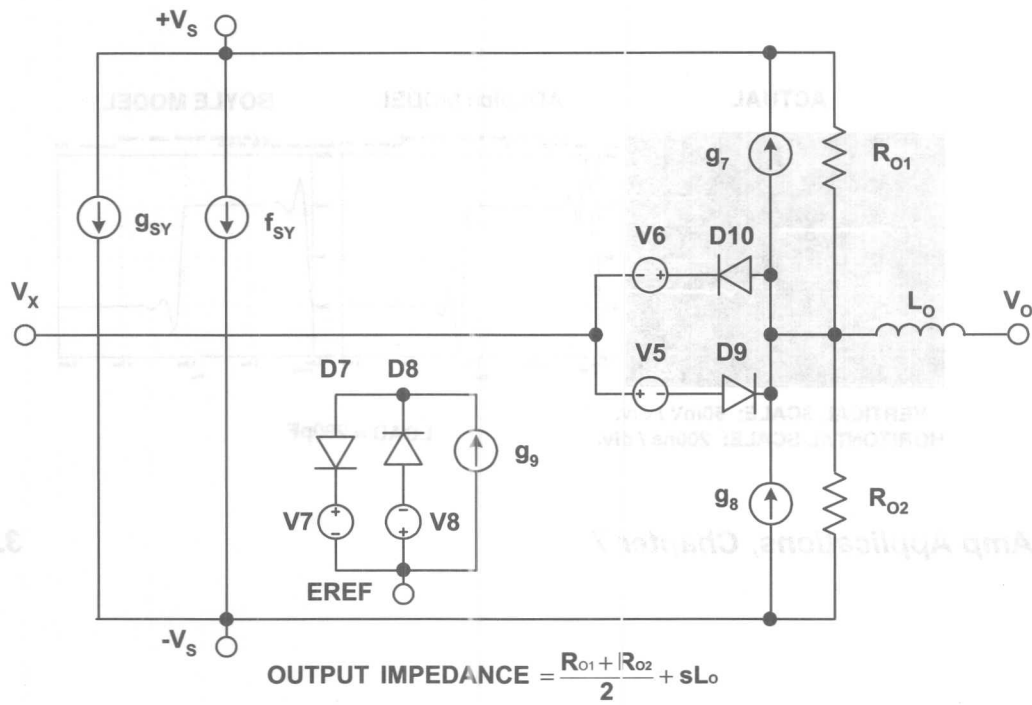
THE FREQUENCY SHAPING STAGES POSSIBLE WITHIN THE ADSpice MODEL



Op Amp Applications, Chapter 7

3.52

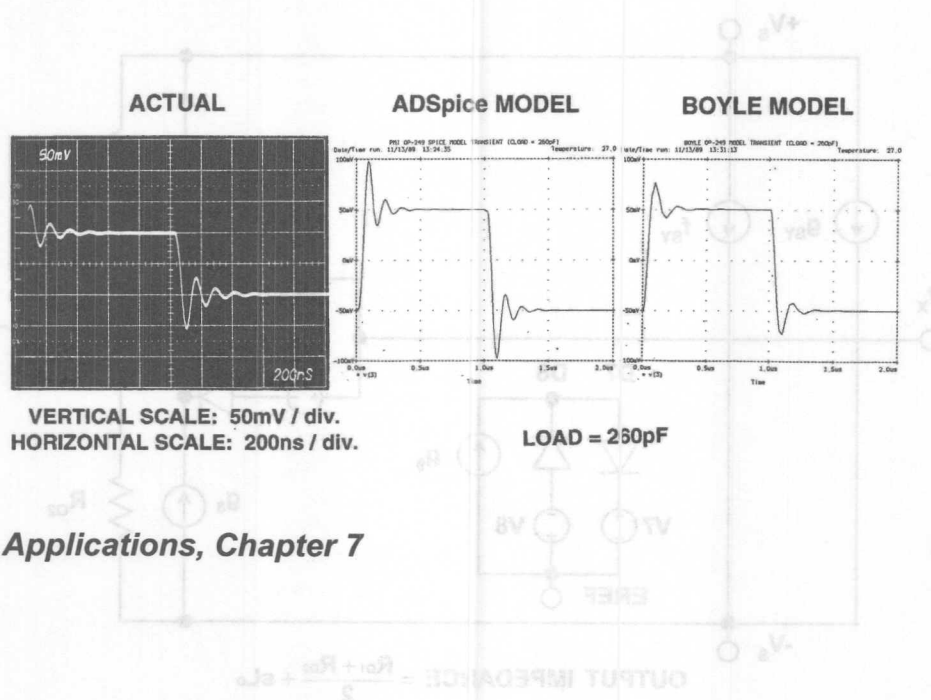
GENERAL-PURPOSE MACROMODEL OUTPUT STAGE



Op Amp Applications, Chapter 7

3.53

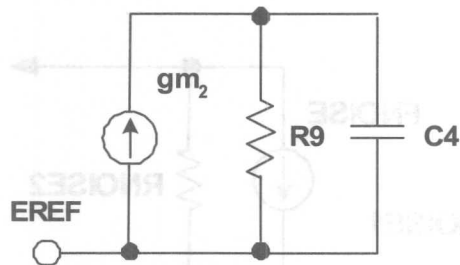
A PULSE RESPONSE COMPARISON OF AN OP249 FOLLOWER (LEFT) MODEL FAVORS THE ADSpice MODEL IN TERMS OF FIDELITY (CENTER), BUT NOT THE BOYLE (RIGHT)



Op Amp Applications, Chapter 7

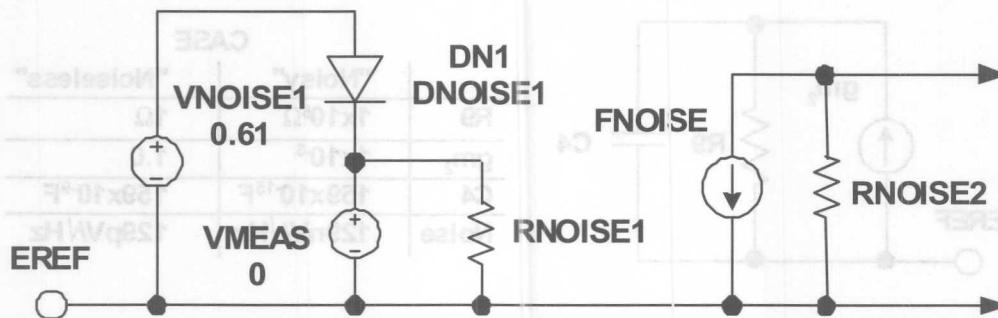
3.54

TOWARDS ACHIEVING LOW NOISE OPERATION, A FIRST DESIGN STEP IS THE REDUCTION OF POLE/ZERO CELL IMPEDANCES TO LOW VALUES



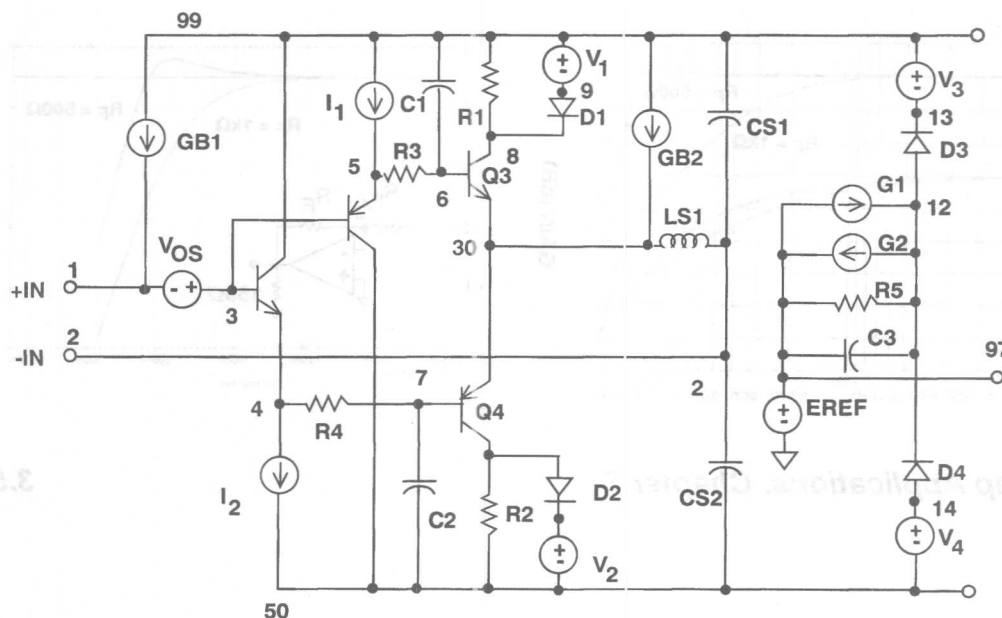
CASE		
	"Noisy"	"Noiseless"
R9	1x10 ⁶ Ω	1Ω
gm ₂	1x10 ⁻⁶	1.0
C4	159x10 ⁻¹⁵ F	159x10 ⁻⁹ F
Noise	129nV/√Hz	129pV/√Hz

A BASIC SPICE NOISE GENERATOR IS FORMED WITH DIODES, RESISTORS, AND CONTROLLED SOURCES



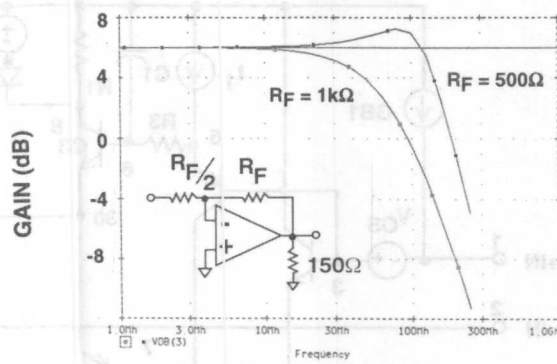
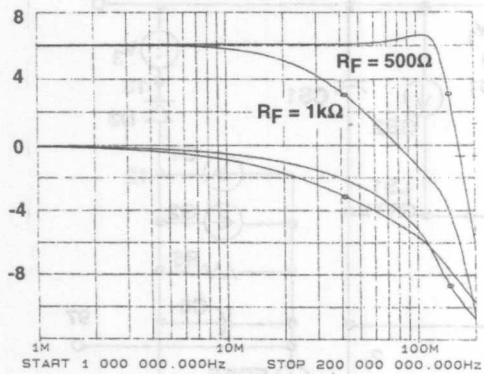
Op Amp Applications, Chapter 7

3.56



3.57

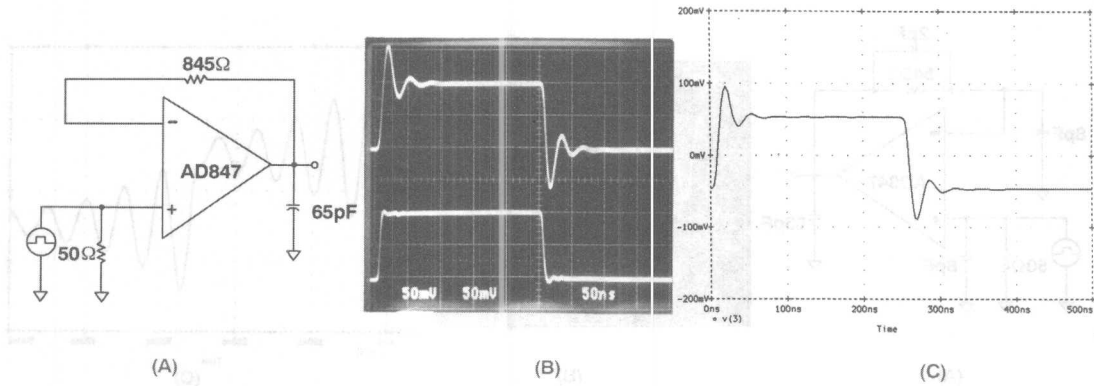
COMPARISON OF A REAL AD811 CURRENT FEEDBACK OP AMP (LEFT)
WITH MACROMODEL (RIGHT) SHOWS SIMILAR CHARACTERISTICS
AS FEEDBACK RESISTANCE IS VARIED



Op Amp Applications, Chapter 7

3.58

WITH CARE AND LOW PARASITIC EFFECTS IN THE PCB LAYOUT, RESULTS OF LAB TESTING (CENTER) AND SIMULATION (RIGHT) CAN CONVERGE

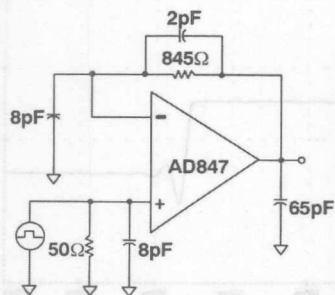


Op Amp Applications, Chapter 7

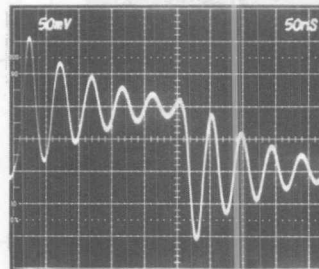
3.59

■ OP AMP APPLICATIONS SEMINAR

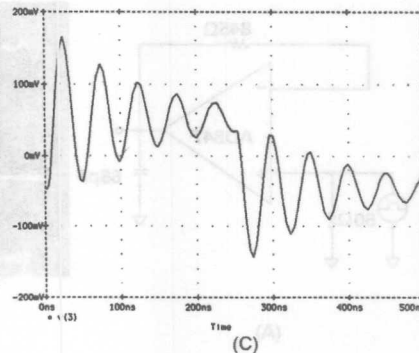
WITHOUT LOW PARASITICS, LAB TESTING RESULTS (CENTER)
AND PARALLEL SIMULATION (RIGHT) STILL SHOW CONVERGENCE—
WITH A POORLY DAMPED RESPONSE



(A)



(B)

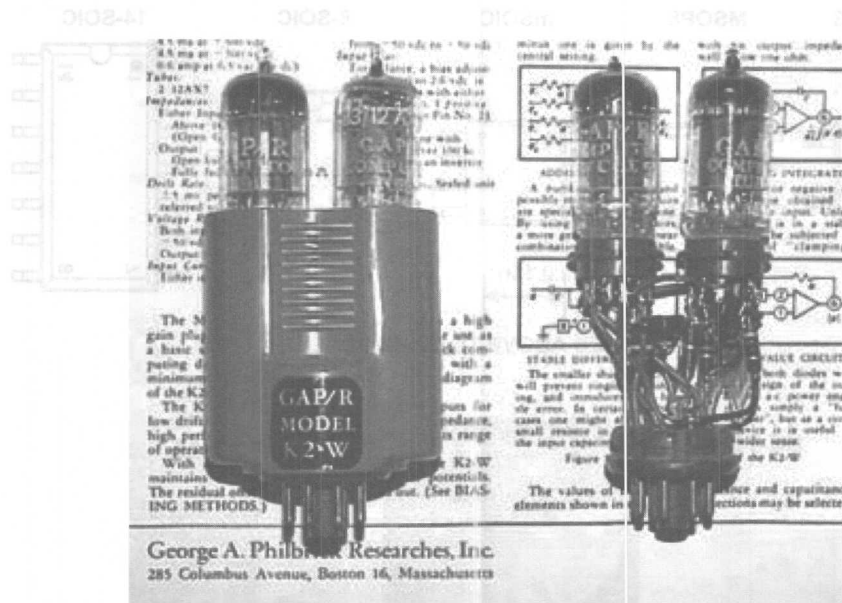


(C)

Op Amp Applications, Chapter 7

3.60

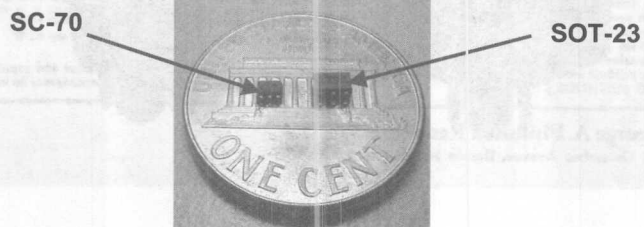
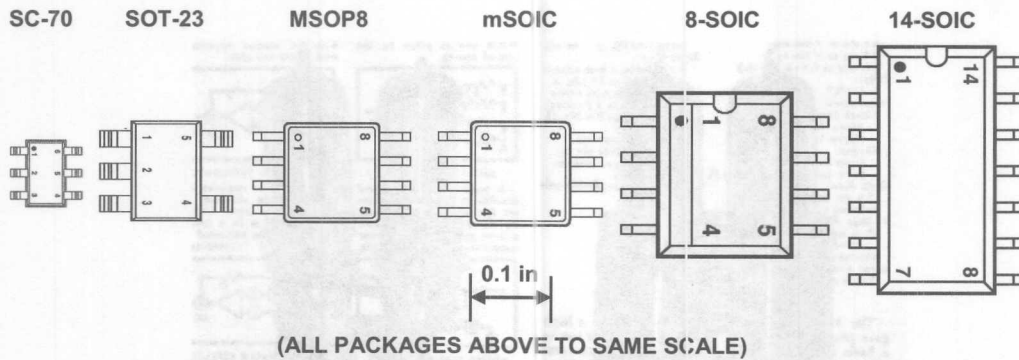
THESE CIRCUITS WERE EASY TO BREADBOARD (EXCEPT FOR THE 300V DC!)



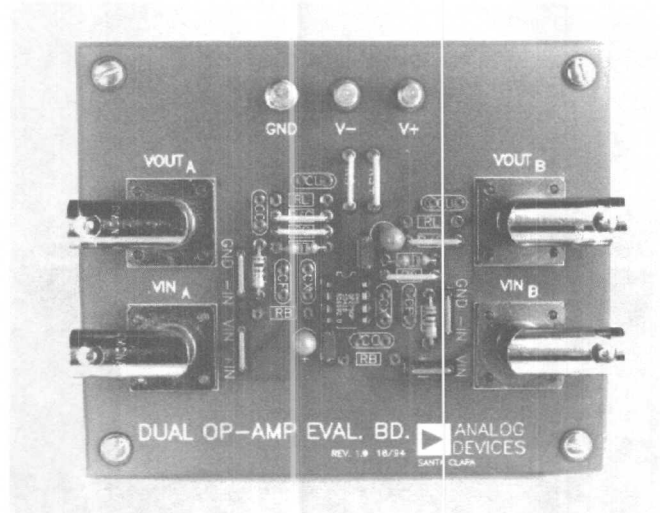
Op Amp Applications, Chapter 7

3.61

SMALL PACKAGE SIZES PRESENT MAJOR DIFFICULTIES IN BREADBOARDING



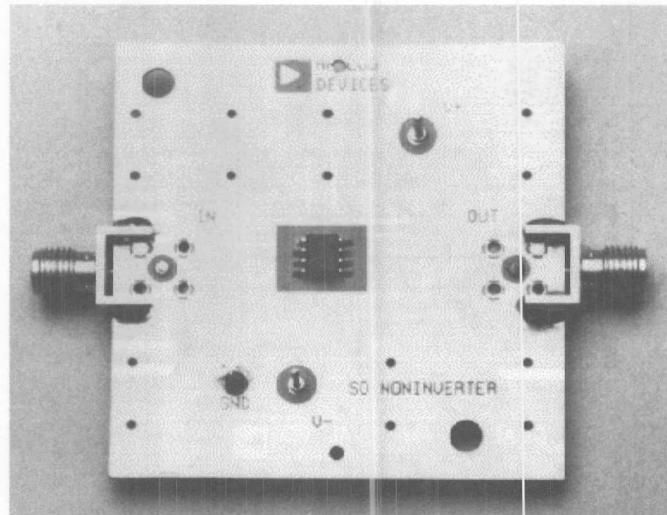
**A GENERAL PURPOSE OP AMP EVALUATION BOARD ALLOWS FAST,
EASY CONFIGURATION OF LOW FREQUENCY OP AMP CIRCUITS**



Op Amp Applications, Chapter 7

3.63

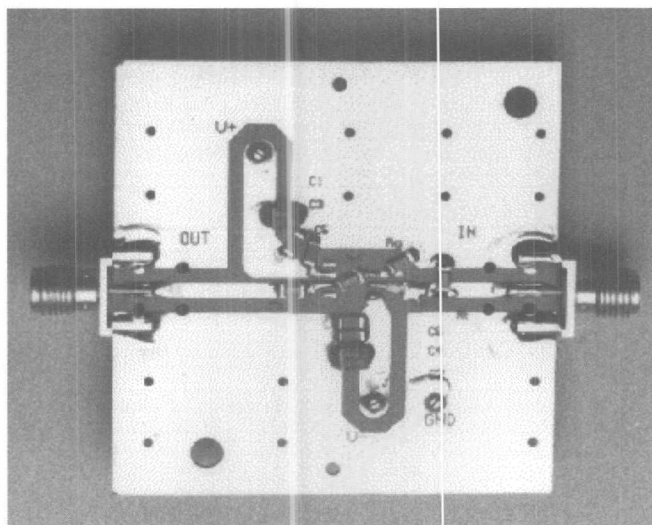
THE AD8001 EVALUATION BOARD USES A LARGE AREA GROUND
PLANE AND MINIMAL PARASITIC CAPACITANCE (TOP VIEW)



Op Amp Applications, Chapter 7

3.64

A HIGH SPEED OP AMP SUCH AS THE AD8001 REQUIRES A DEDICATED EVALUATION BOARD WITH SUITABLE GROUND PLANES AND DECOUPLING (BOTTOM VIEW)



Op Amp Applications, Chapter 7

3.65

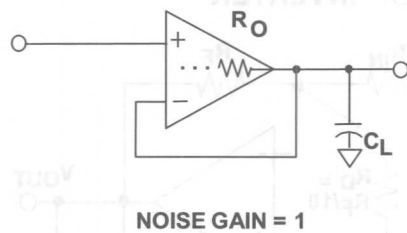
OP AMP APPLICATIONS SEMINAR

1. History, Basics, Design Aids, Filters
2. Specialty Amplifiers, Using Op Amps with Data Converters
3. Hardware and Housekeeping Design Techniques
4. **Signal Amplifiers, Sensor Signal Conditioning**

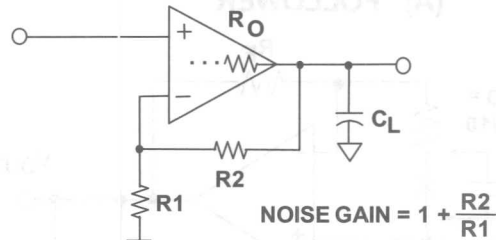
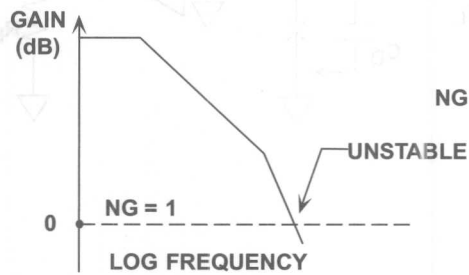
OP AMP APPLICATIONS SEMINAR

1. History, Basics, Design Aids, Filters
2. Specialty Amplifiers, Using Op Amps with Data Converters
3. Hardware and Housekeeping Design Techniques
4. Signal Amplifiers, Sensor Signal Conditioning

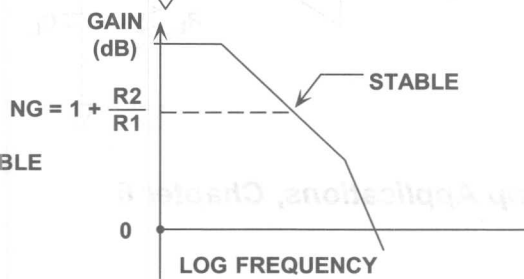
EFFECT OF CAPACITIVE LOADING ON OP AMP STABILITY



NOISE GAIN = 1

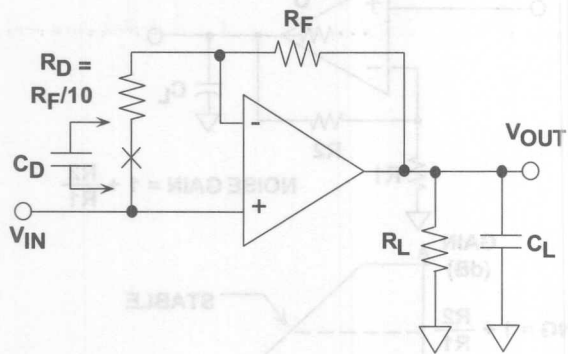


NOISE GAIN = $1 + \frac{R_2}{R_1}$

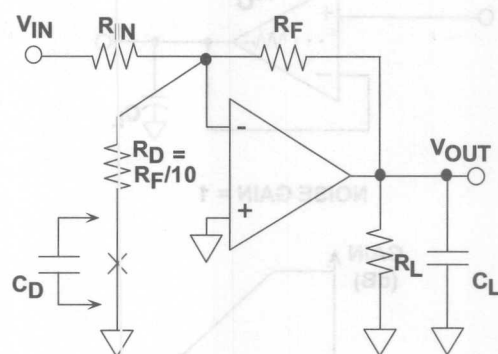


RAISING NOISE GAIN (DC OR AC) FOR FOLLOWER (A) OR INVERTER (B) STABILITY

(A) FOLLOWER



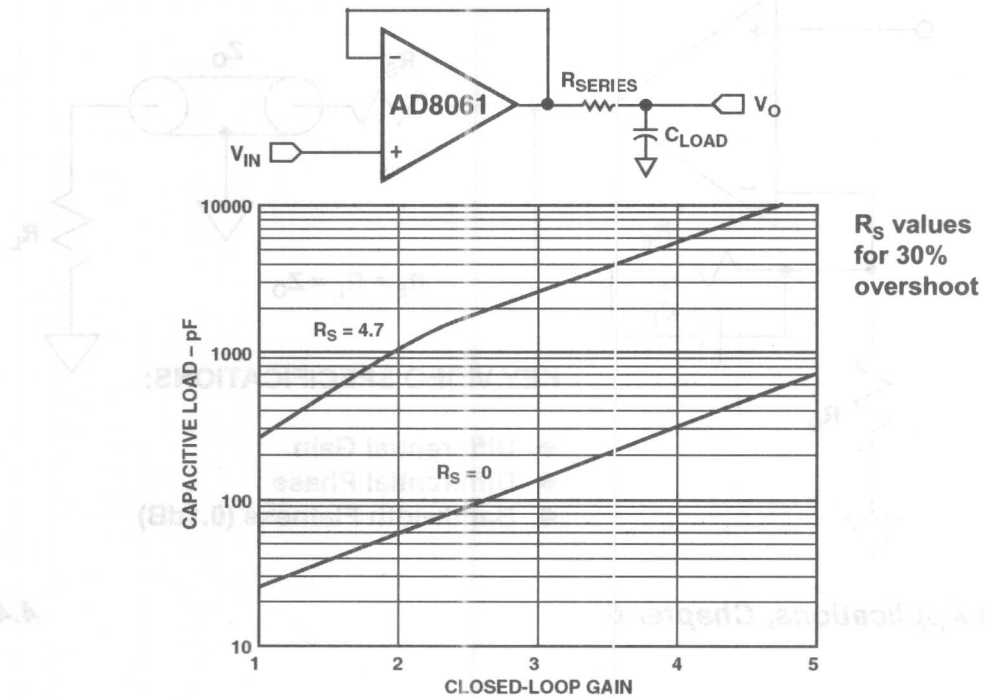
(B) INVERTER



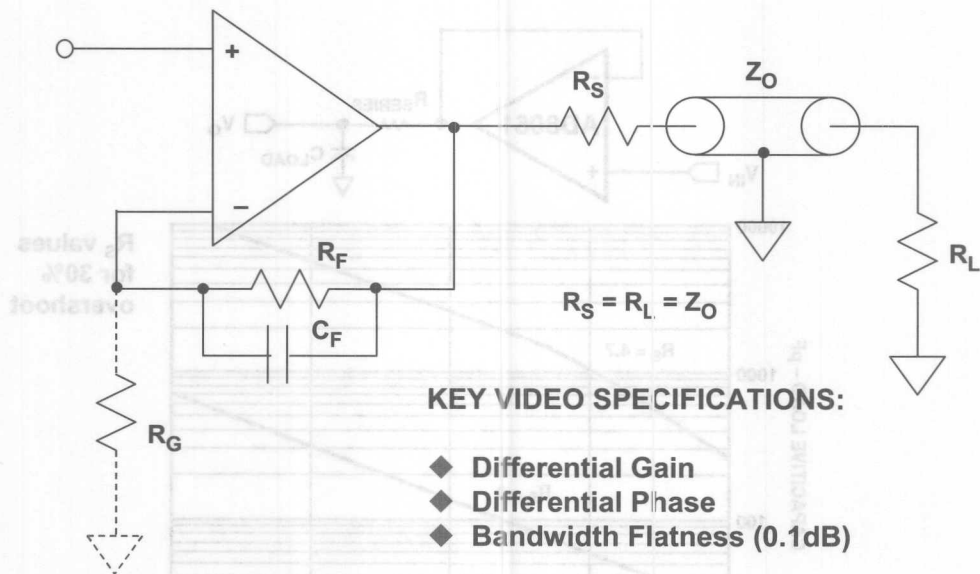
Op Amp Applications, Chapter 6

4.2

DRIVING CAPACITIVE LOADS



VIDEO TRANSMISSION LINE DRIVERS

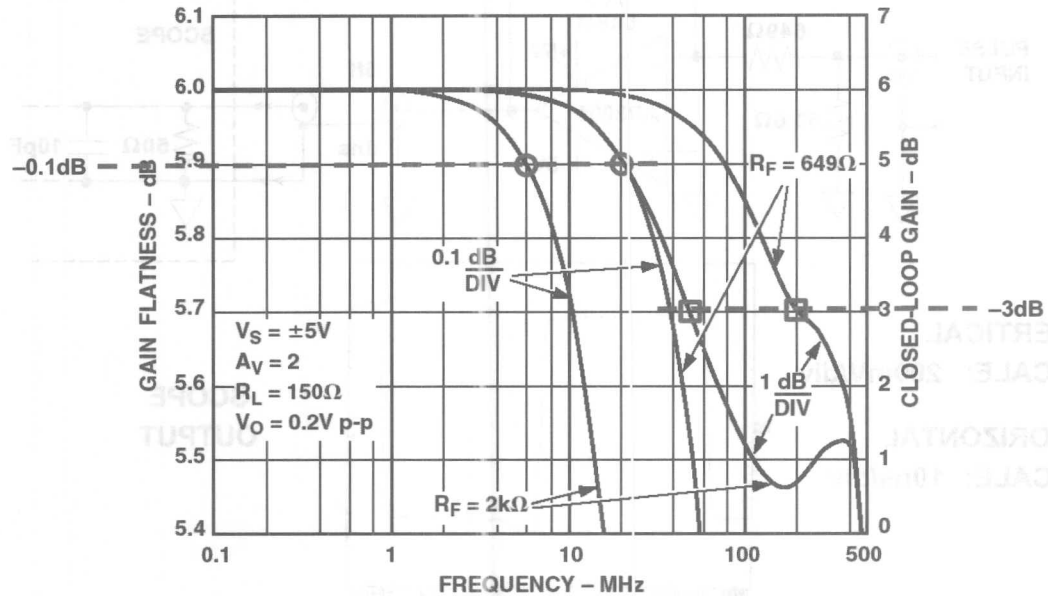


Op Amp Applications, Chapter 6

4.4

AD8072/73 DUAL/TRIPLE VIDEO BUFFERS

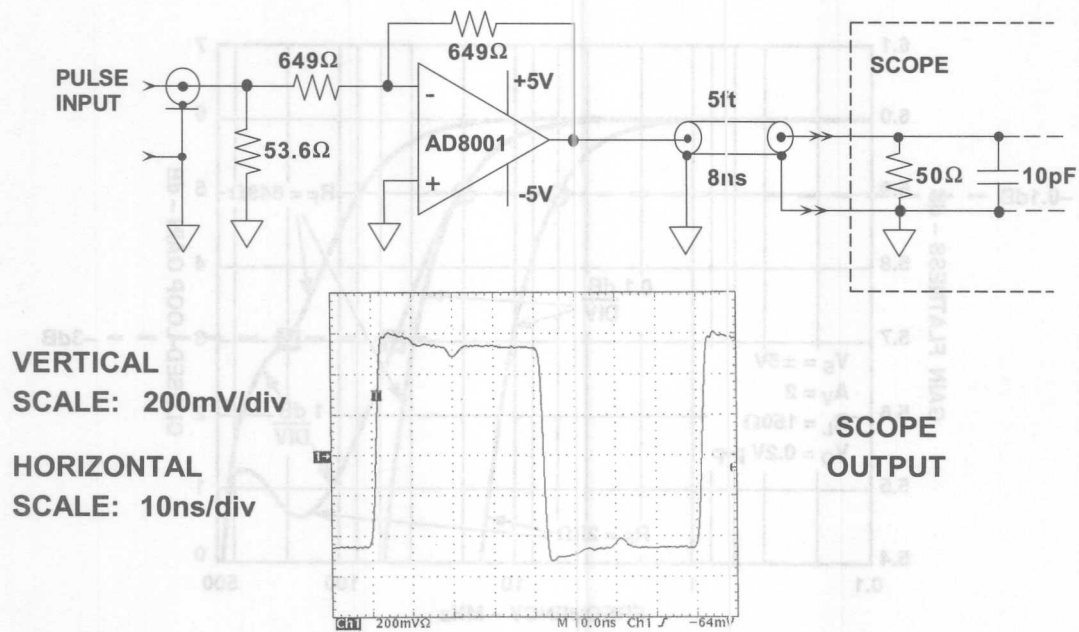
GAIN AND GAIN FLATNESS, $G = +2$, $R_L = 150\Omega$



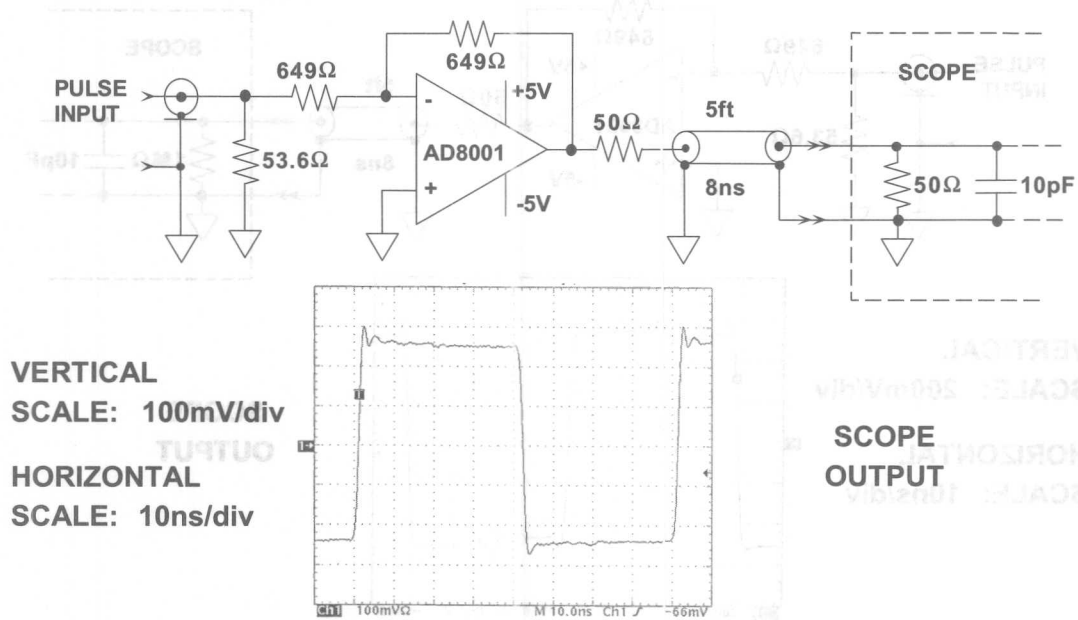
Op Amp Applications, Chapter 6

4.5

PULSE RESPONSE OF AD8001 DRIVING 5 FEET OF LOAD-ONLY TERMINATED 50Ω COAXIAL CABLE



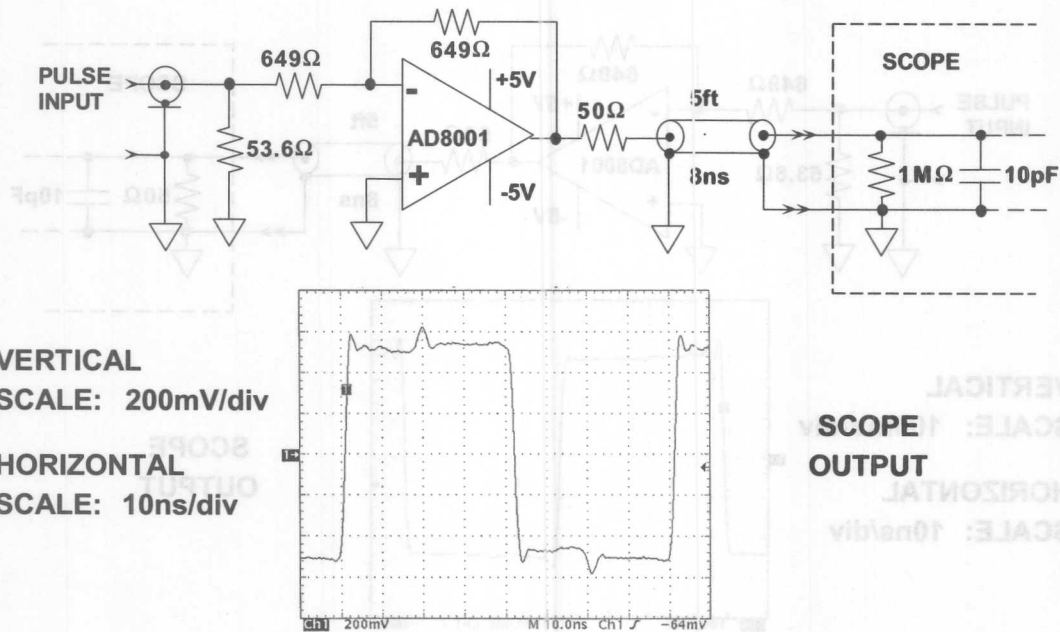
PULSE RESPONSE OF AD8001 DRIVING 5 FEET OF SOURCE AND LOAD TERMINATED 50Ω COAXIAL CABLE



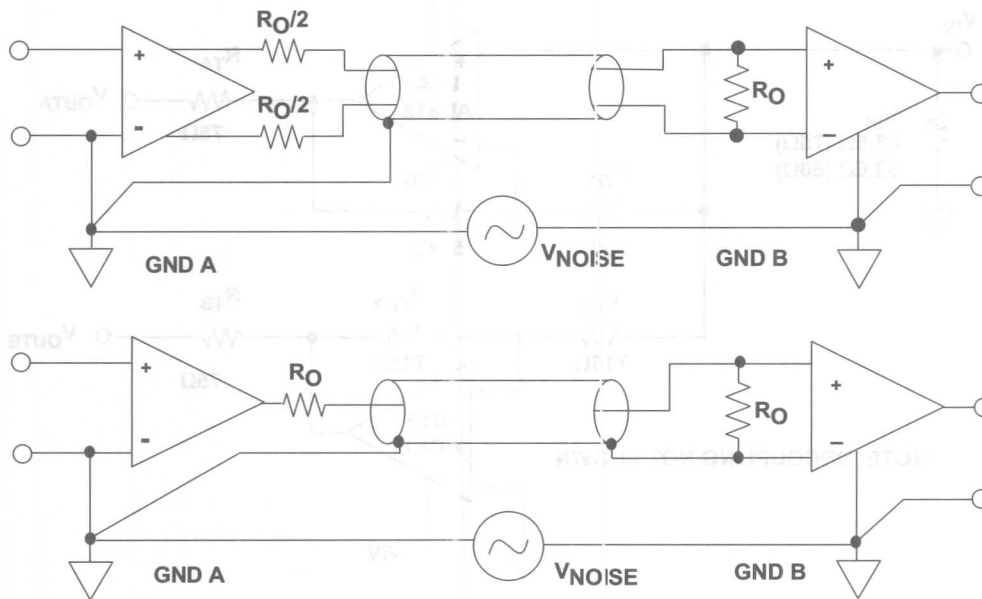
Op Amp Applications, Chapter 6

4.7

PULSE RESPONSE OF AD8001 DRIVING 5 FEET OF SOURCE-ONLY TERMINATED 50Ω COAXIAL CABLE



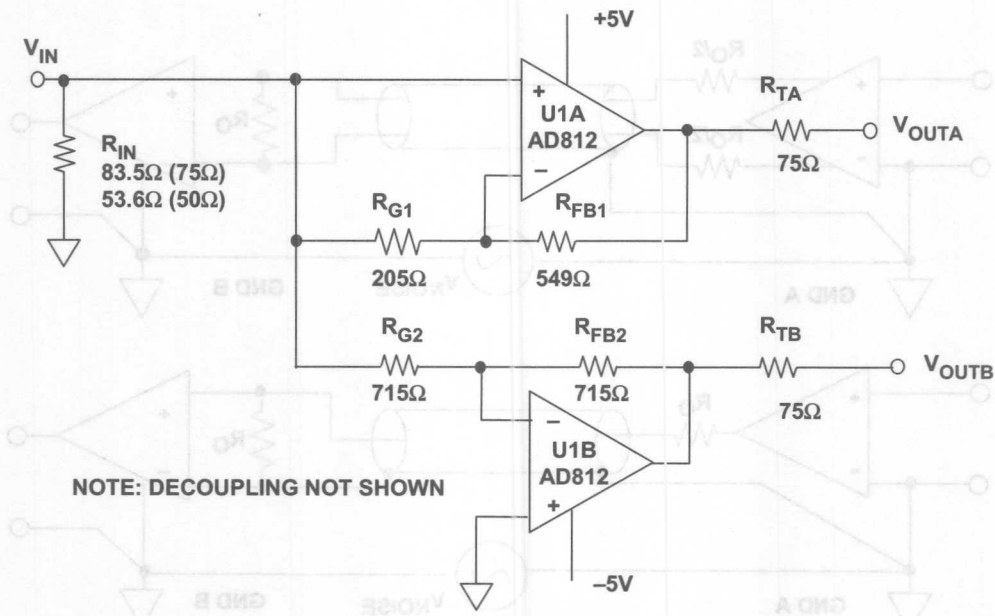
TWO APPROACHES TO DIFFERENTIAL LINE DRIVING AND RECEIVING



Op Amp Applications, Chapter 6

4.9

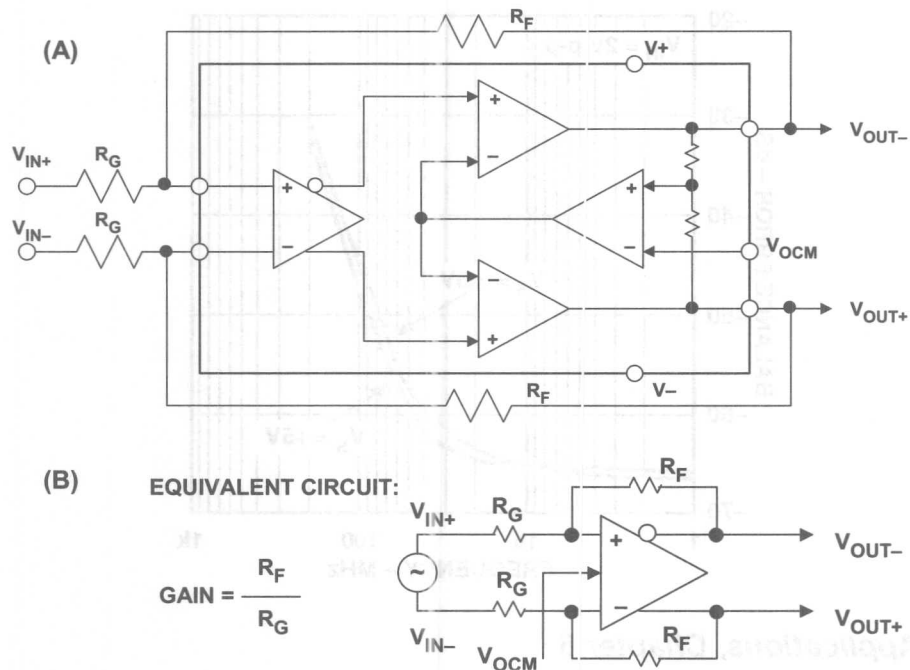
DIFFERENTIAL DRIVER USING AN INVERTER AND A FOLLOWER



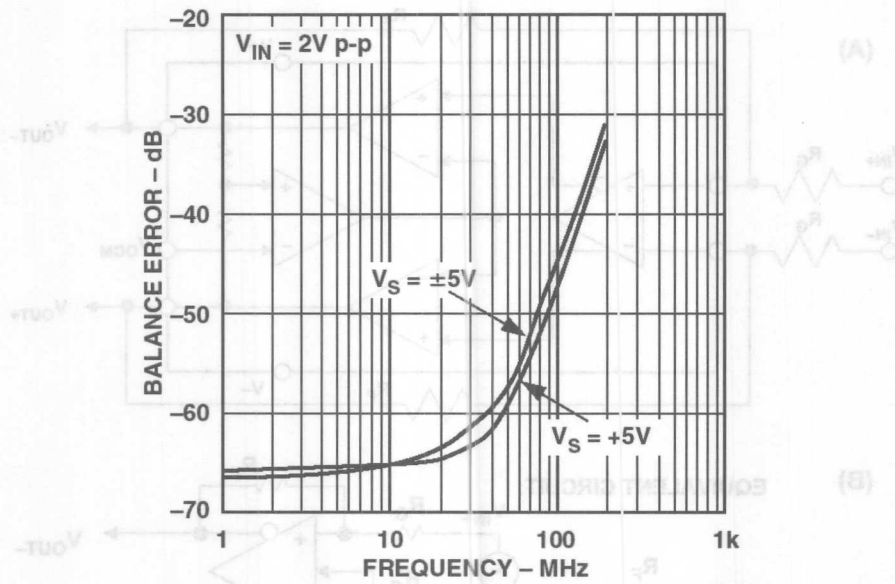
Op Amp Applications, Chapter 6

4.10

AD8138 DIFFERENTIAL DRIVER AMPLIFIER FUNCTIONAL SCHEMATIC (A) AND EQUIVALENT CIRCUIT (B)



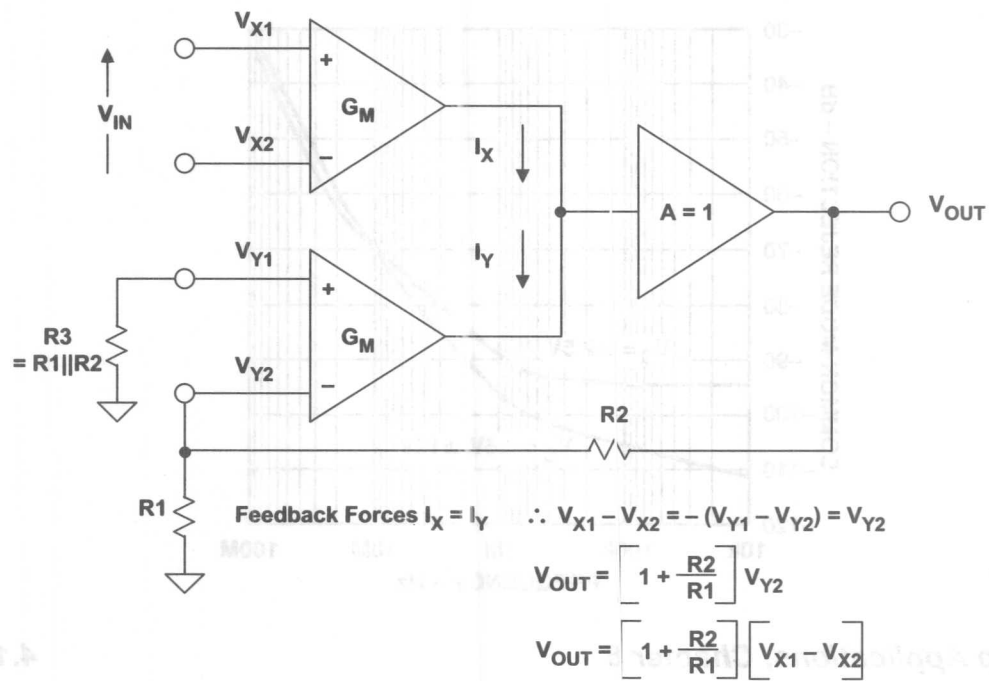
AD8138 OUTPUT BALANCE ERROR VERSUS FREQUENCY



Op Amp Applications, Chapter 6

4.12

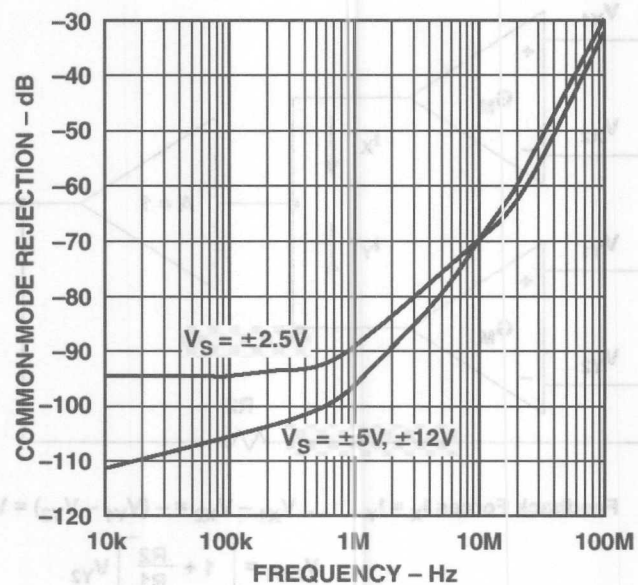
THE AD8129/AD8130 ACTIVE FEEDBACK AMPLIFIER TOPOLOGY



Op Amp Applications, Chapter 6

4.13

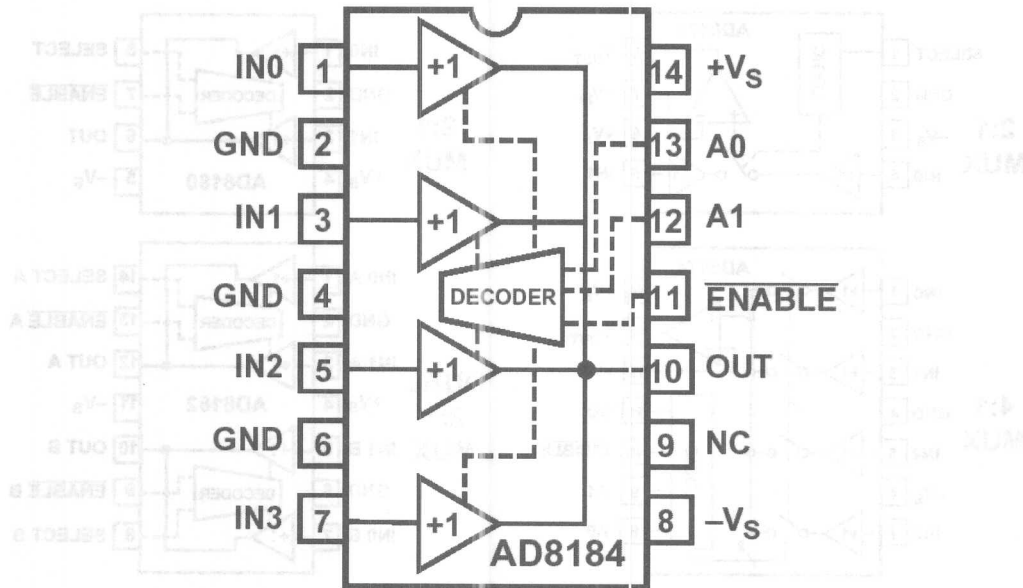
AD8130 COMMON-MODE REJECTION VERSUS FREQUENCY FOR $\pm 2.5V$, $\pm 5V$, AND $\pm 12V$ SUPPLIES



Op Amp Applications, Chapter 6

4.14

AD8184 4:1 VIDEO MULTIPLEXER

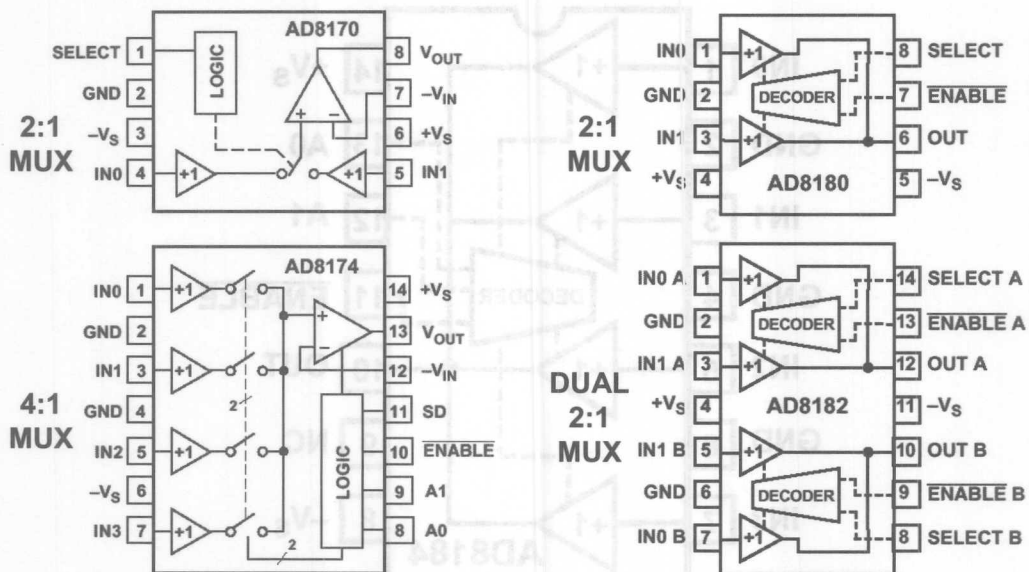


NC = NO CONNECT

Op Amp Applications, Chapter 6

4.15

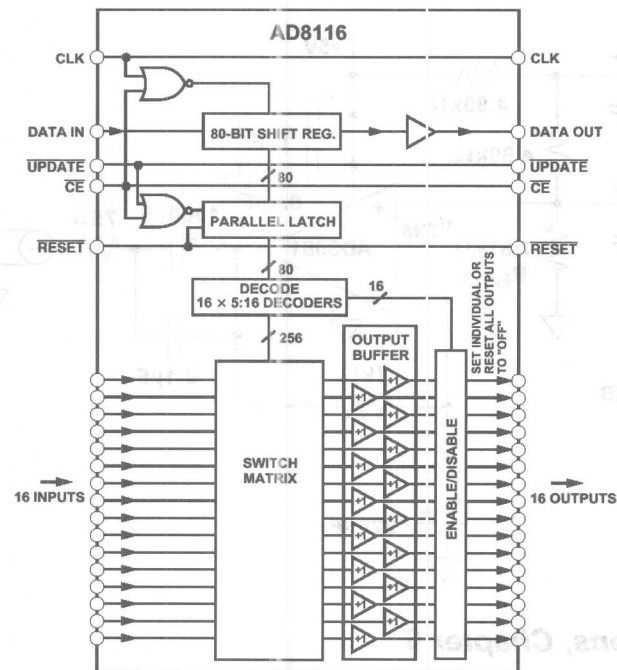
AD8170/8174/8180/8182 BIPOLAR VIDEO MULTIPLEXERS



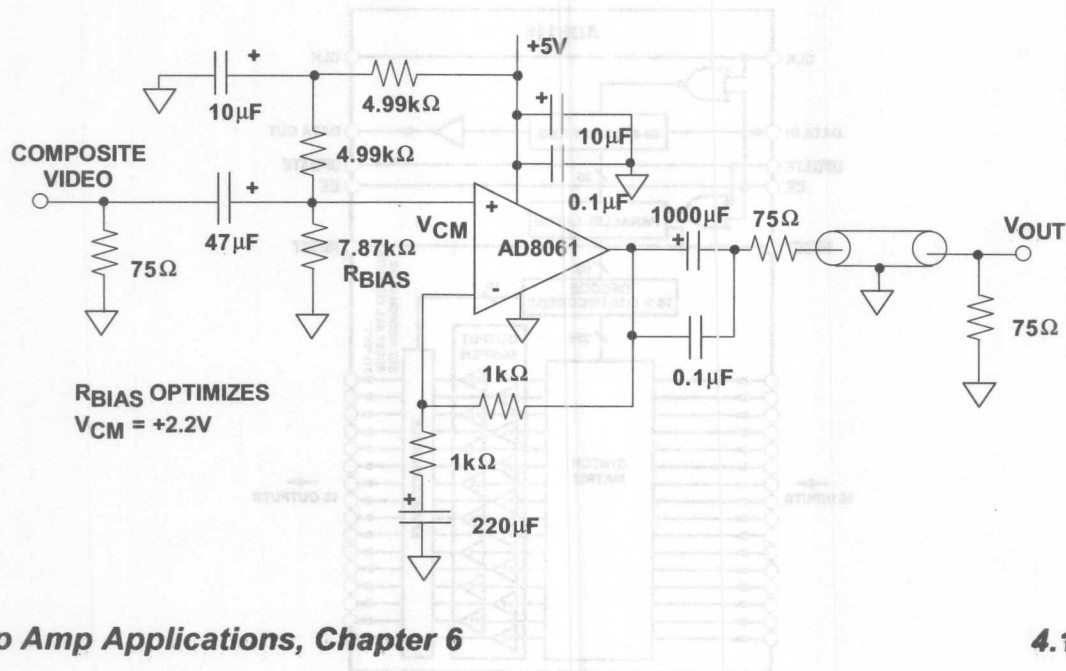
Op Amp Applications, Chapter 6

4.16

AD8116 16×16 200MHZ BUFFERED VIDEO CROSSPOINT SWITCH



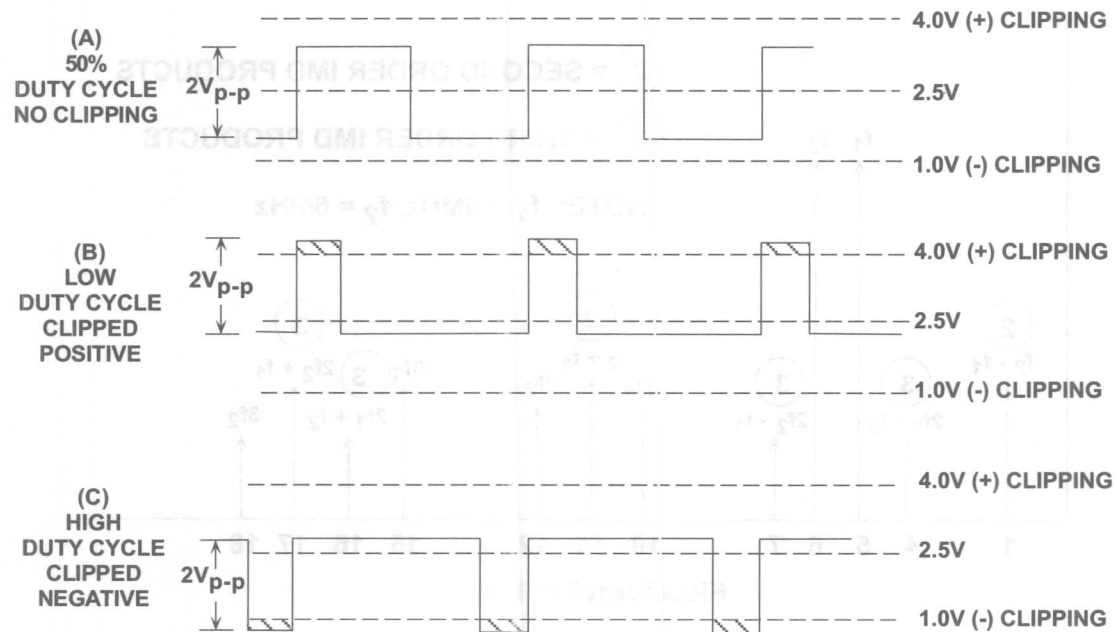
SINGLE-SUPPLY AC COUPLED COMPOSITE VIDEO LINE DRIVER HAS $\Delta G = 0.06\%$ AND $\Delta\phi = 0.06^\circ$



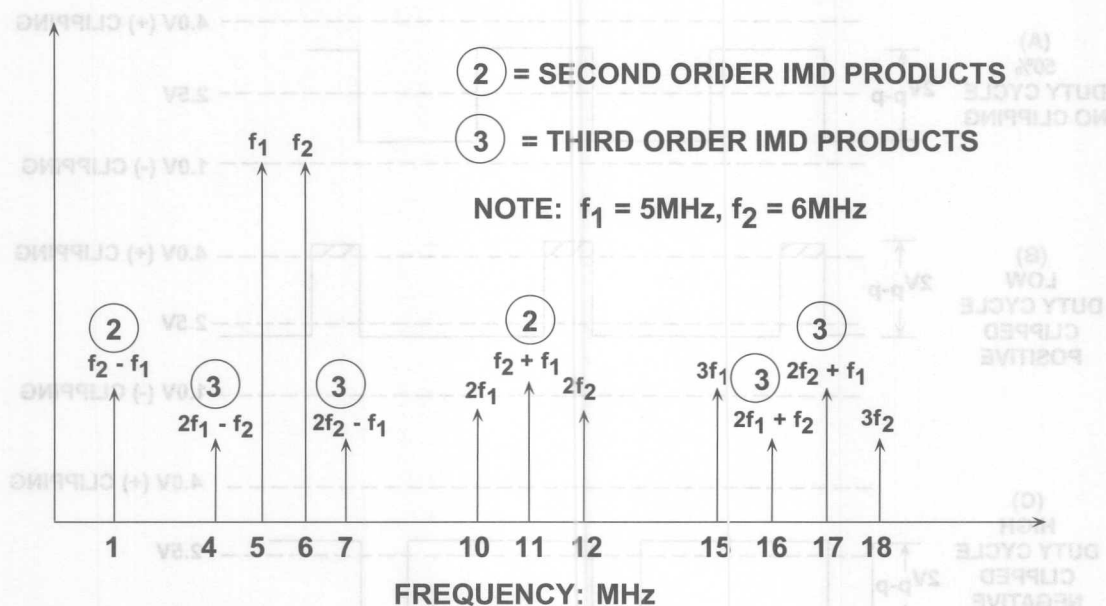
Op Amp Applications, Chapter 6

4.18

WAVEFORM DUTY CYCLE TAXES HEADROOM IN AC COUPLED SINGLE-SUPPLY OP AMPS



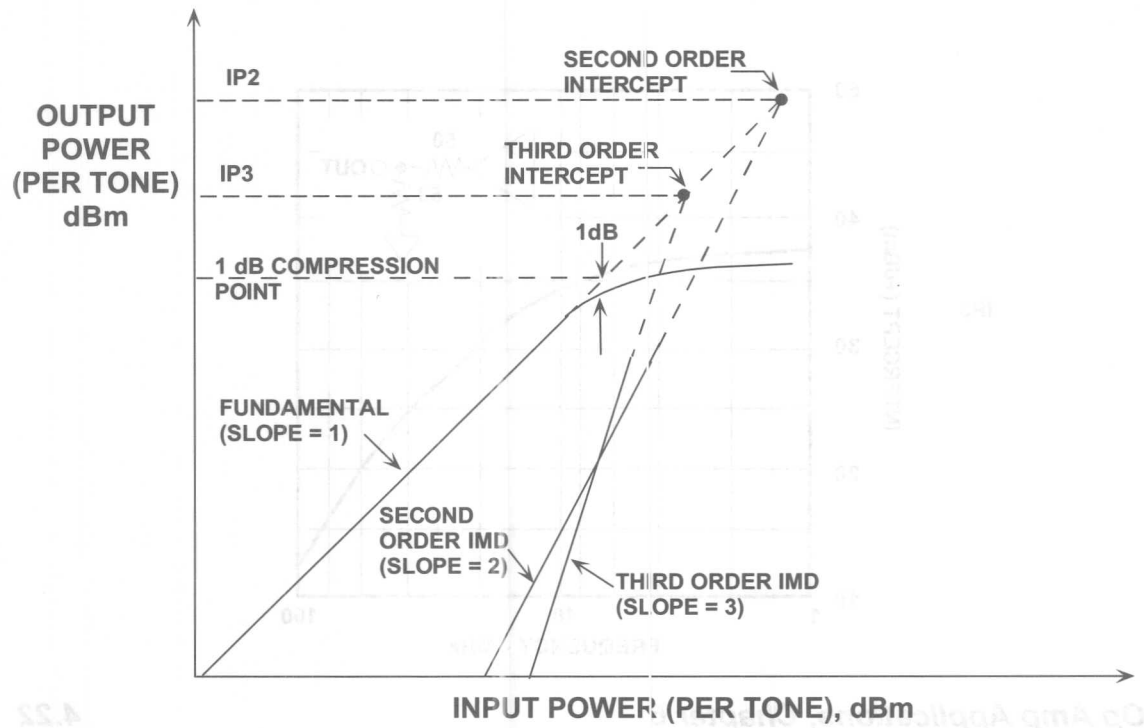
SECOND AND THIRD ORDER INTERMODULATION DISTORTION PRODUCTS



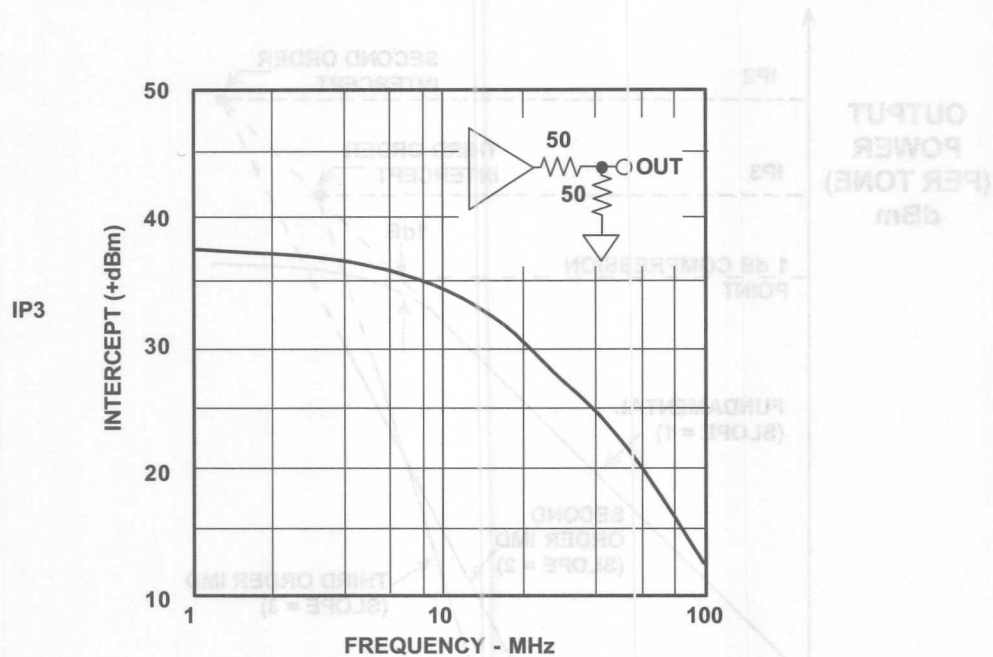
Op Amp Applications, Chapter 6

4.20

INTERCEPT POINTS AND 1dB COMPRESSION POINT



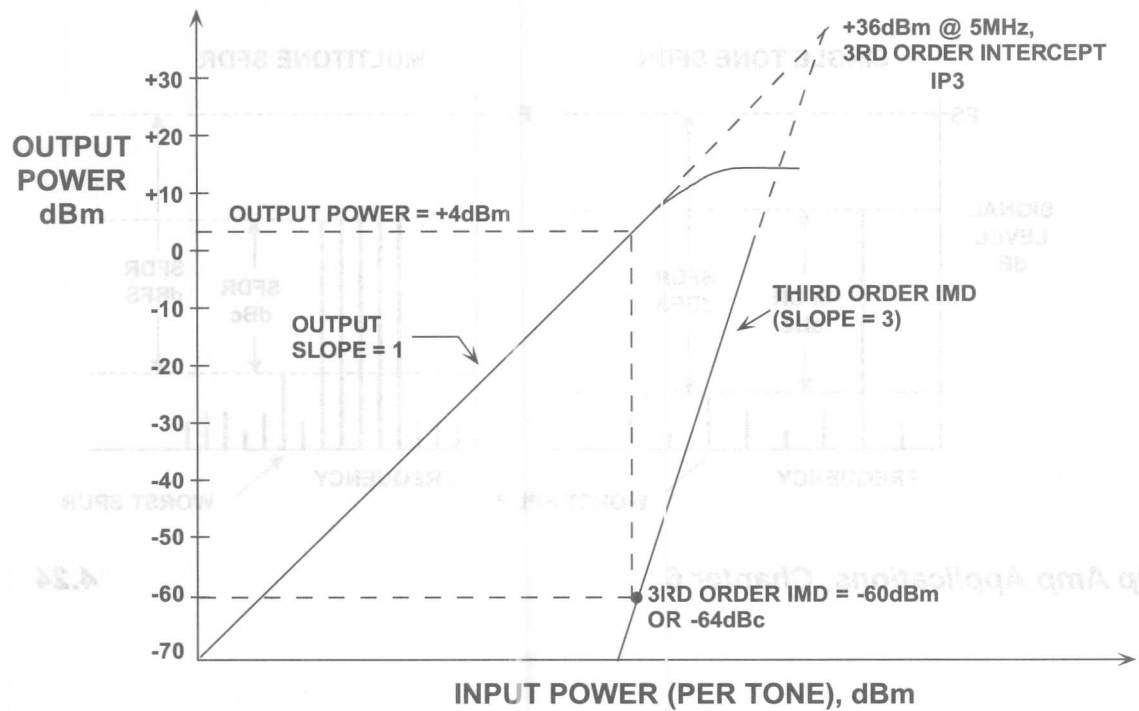
THIRD ORDER INTERCEPT POINT (IP3) VERSUS FREQUENCY FOR A LOW DISTORTION AMPLIFIER



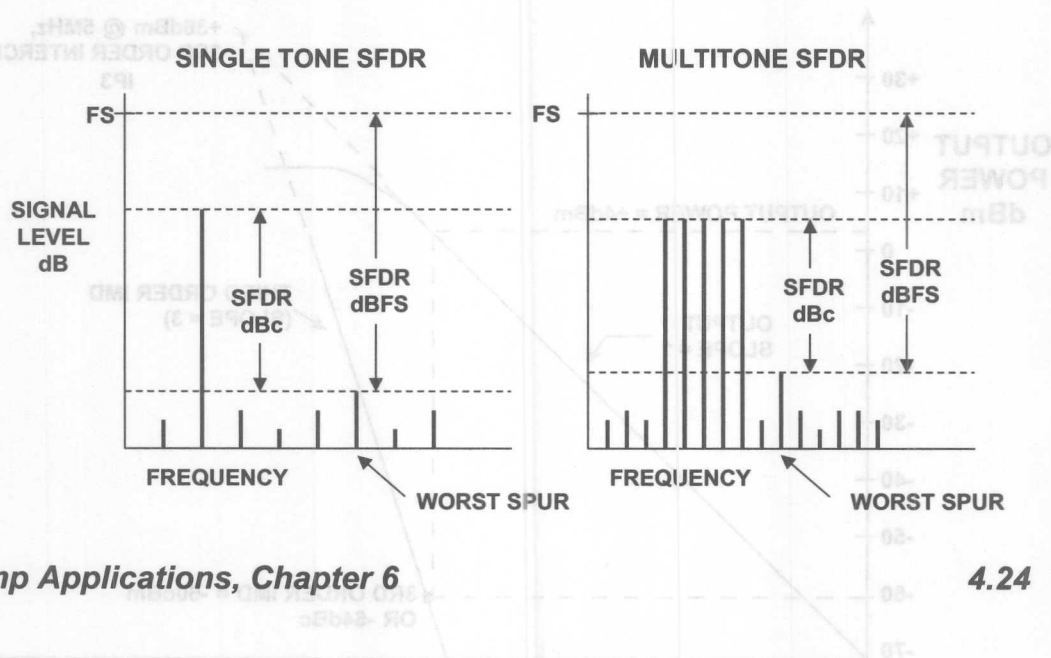
Op Amp Applications, Chapter 6

4.22

USING IP3 TO CALCULATE THE THIRD-ORDER IMD PRODUCT AMPLITUDE



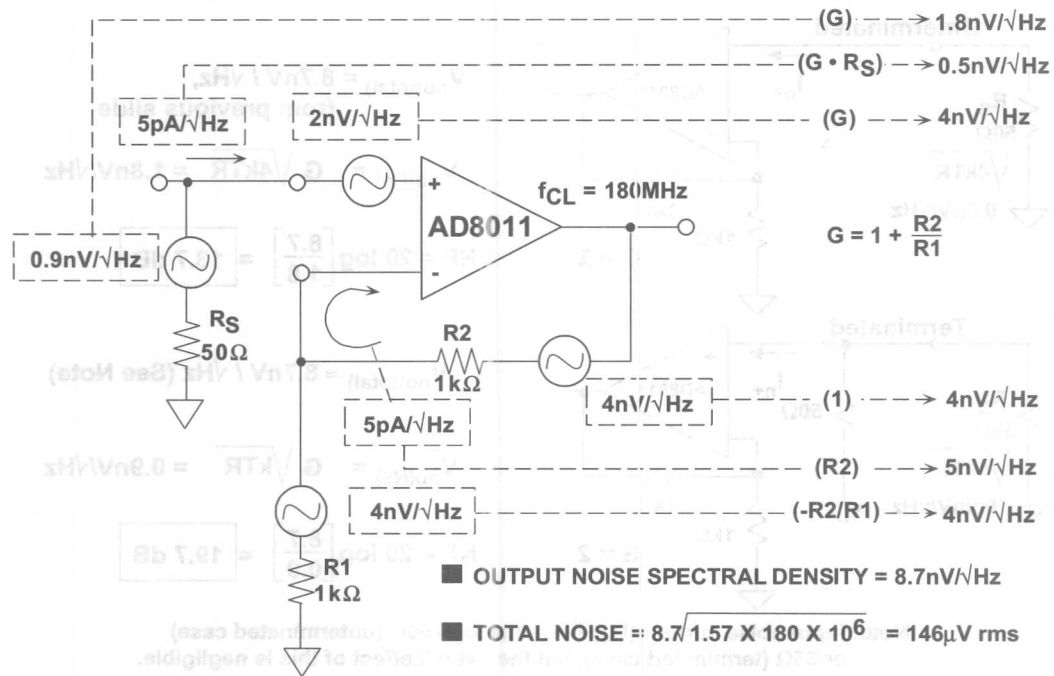
SPURIOUS FREE DYNAMIC RANGE (SFDR) IN COMMUNICATIONS SYSTEMS



Op Amp Applications, Chapter 6

4.24

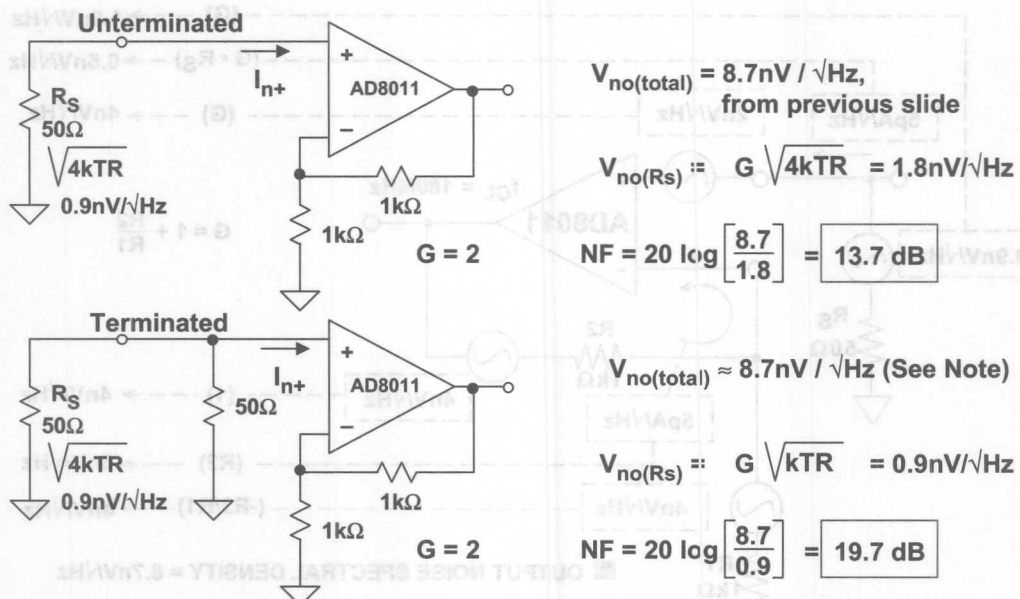
AD8011 OUTPUT NOISE ANALYSIS



Op Amp Applications, Chapter 6

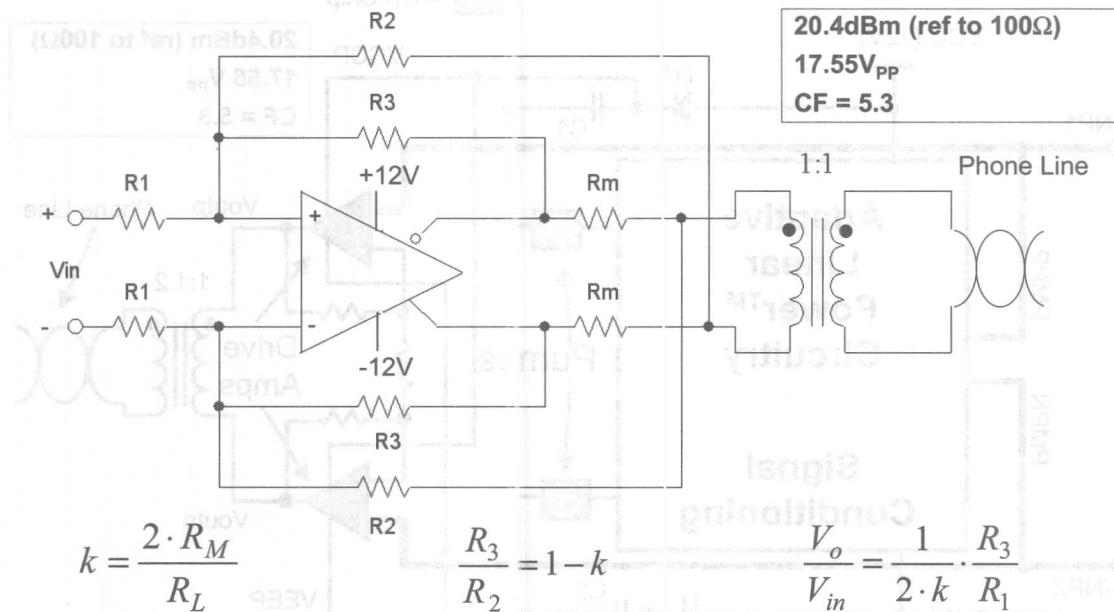
4.25

AD8011 NOISE FIGURE FOR UNTERMINATED AND TERMINATED INPUT CONDITIONS



Note: Input noise current (I_{n+}) flows through 50Ω (unterminated case) or 25Ω (terminated case), but the overall effect of this is negligible.

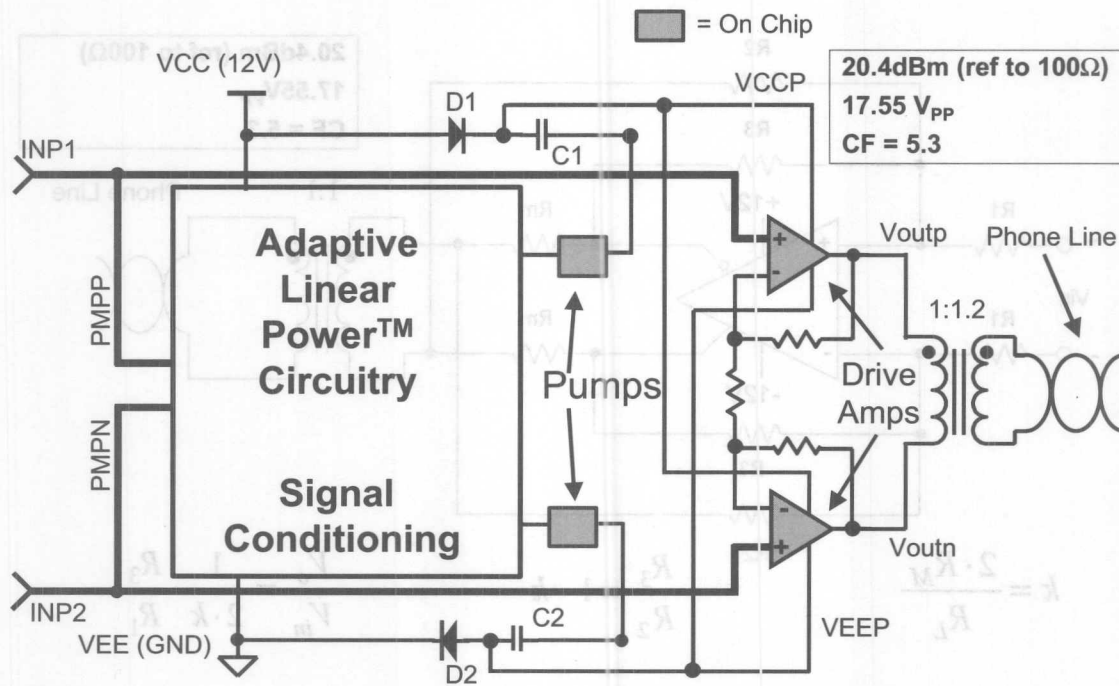
AD8390 FULLY DIFFERENTIAL ADSL CENTRAL OFFICE LINE DRIVER



Op Amp Applications, Chapter 6

4.27

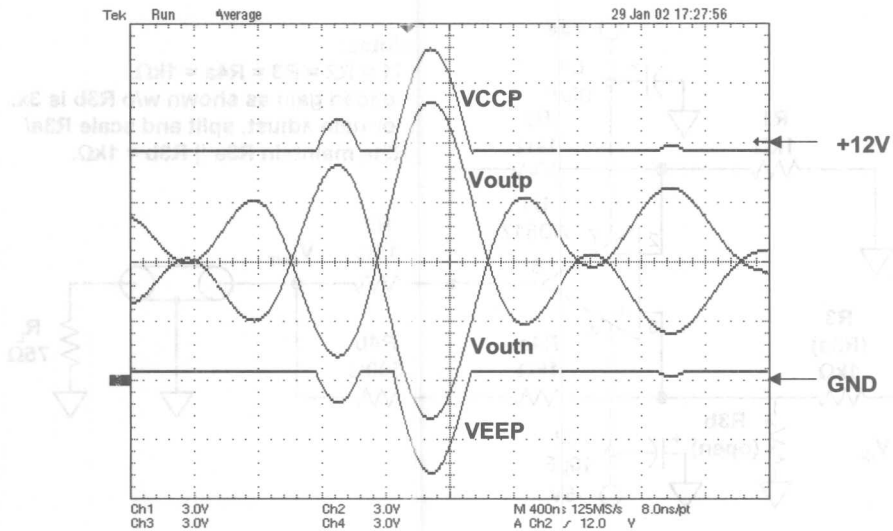
AD8393 ADAPTIVE LINEAR POWER™ +12V CENTRAL OFFICE ADSL LINE DRIVER



Op Amp Applications, Chapter 6

4.28

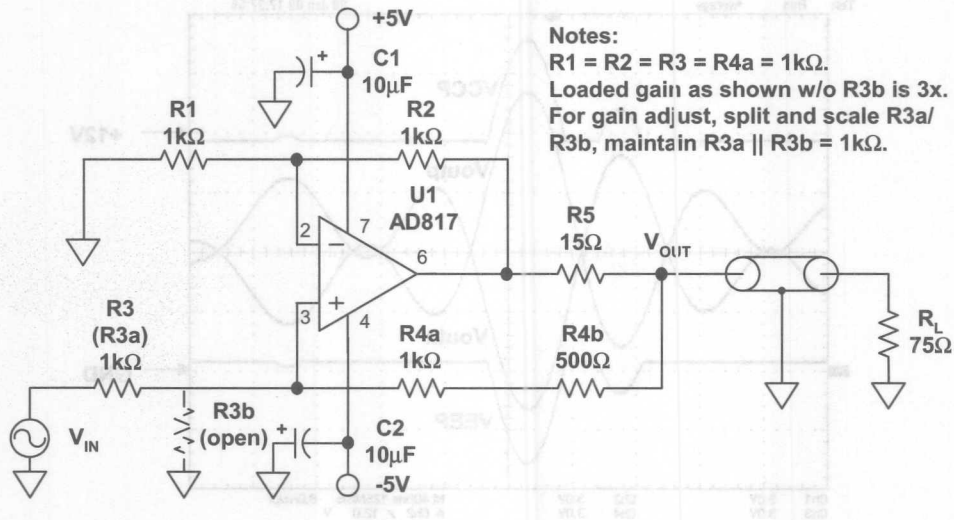
AD8393 - ADAPTIVE LINEAR POWER™ DRIVER CIRCUIT WAVEFORMS



Op Amp Applications, Chapter 6

4.29

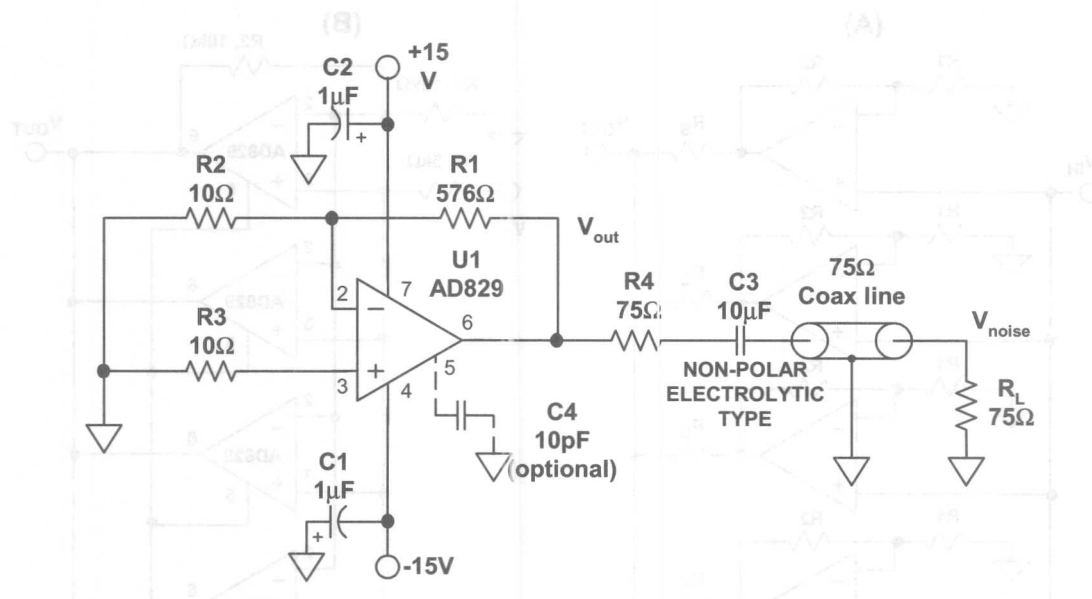
A HIGH EFFICIENCY VIDEO LINE DRIVER



Op Amp Applications, Chapter 6

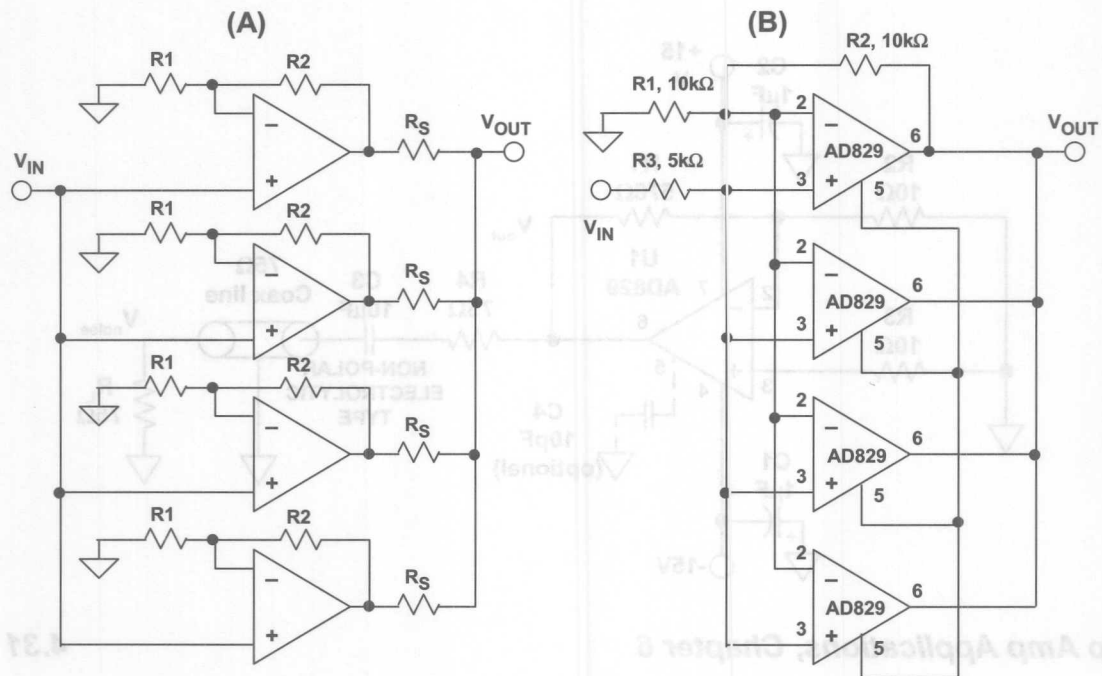
4.30

A SIMPLE WIDEBAND NOISE GENERATOR

*Op Amp Applications, Chapter 6*

4.31

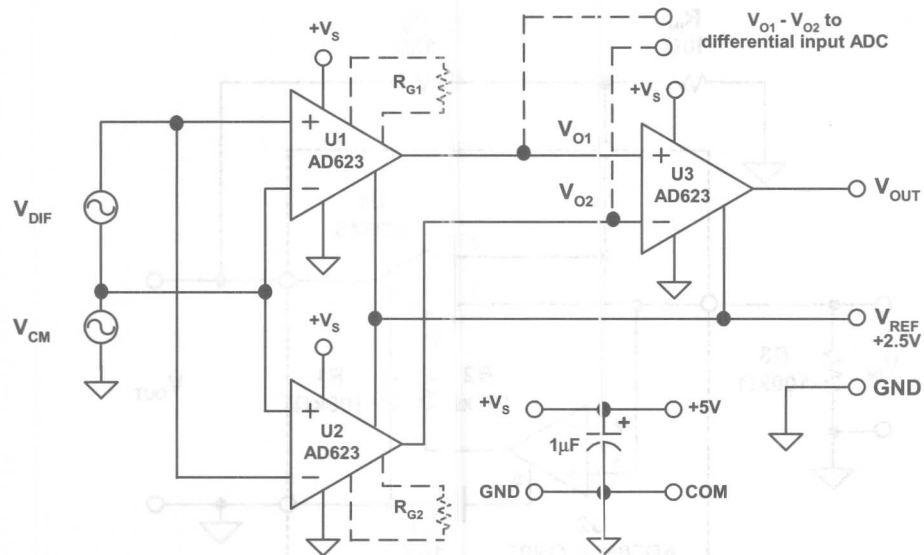
PARALLELED AMPLIFIERS DRIVE LOADS QUIETLY



Op Amp Applications, Chapter 6

4.32

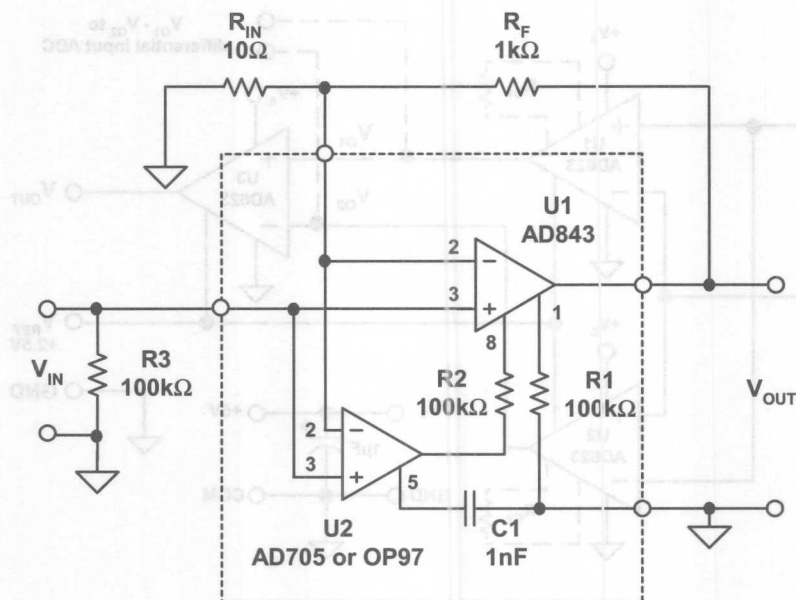
TWO CROSS-COUPLED AND SIMILAR IN-AMP DEVICES FOLLOWED BY A THIRD PROVIDES MUCH INCREASED CMR WITH FREQUENCY



Op Amp Applications, Chapter 6

4.33

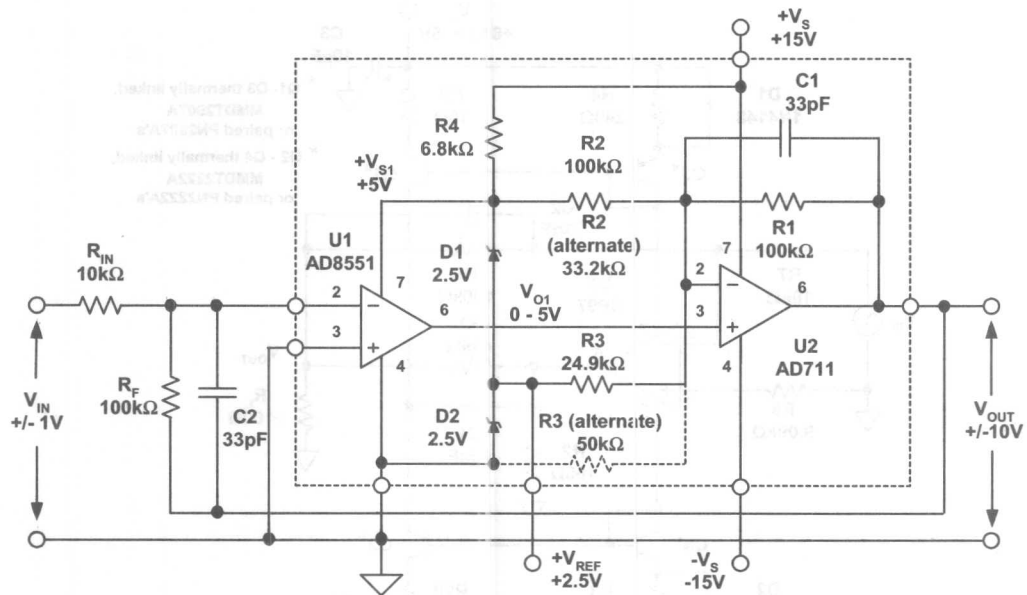
LOW NOISE, LOW DRIFT TWO OP AMP COMPOSITE AMPLIFIER



Op Amp Applications, Chapter 6

4.34

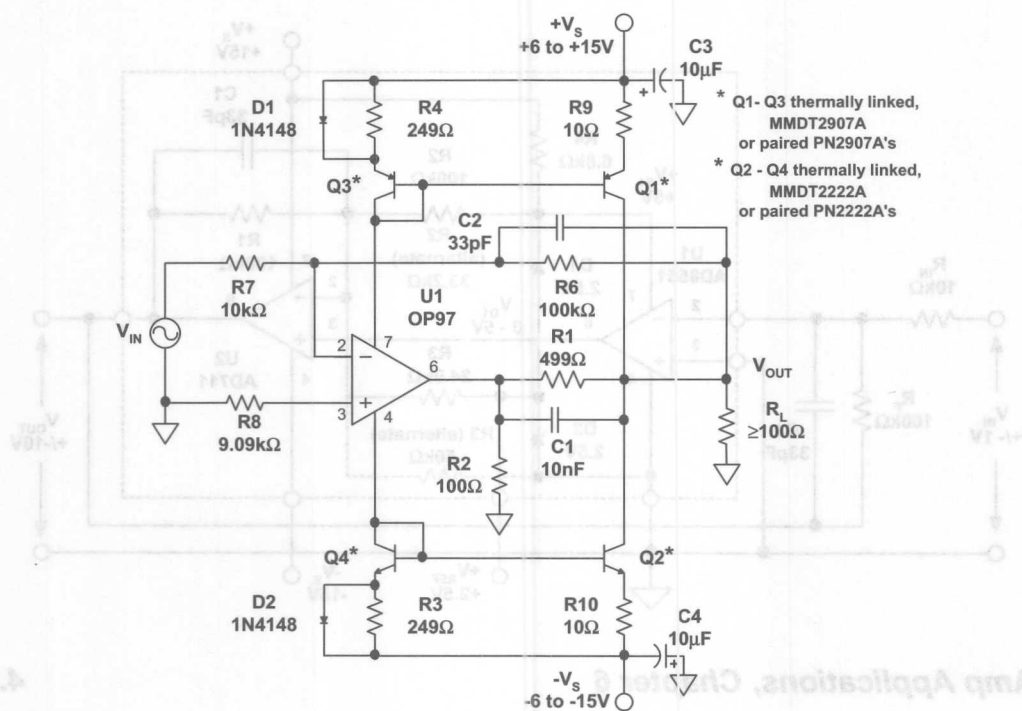
**CHOPPER-STABILIZED 160dB GAIN, LOW VOLTAGE SINGLE-SUPPLY
TO HIGH OUTPUT VOLTAGE COMPOSITE AMPLIFIER**



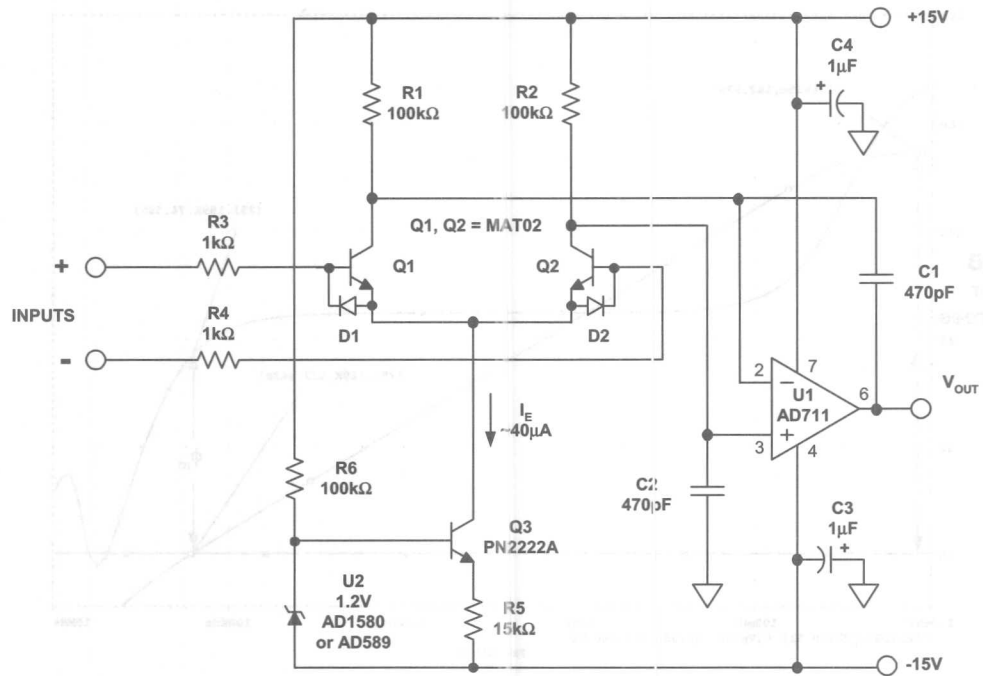
Op Amp Applications, Chapter 6

4.35

VOLTAGE BOOSTED RAIL-RAIL OUTPUT COMPOSITE OP AMP



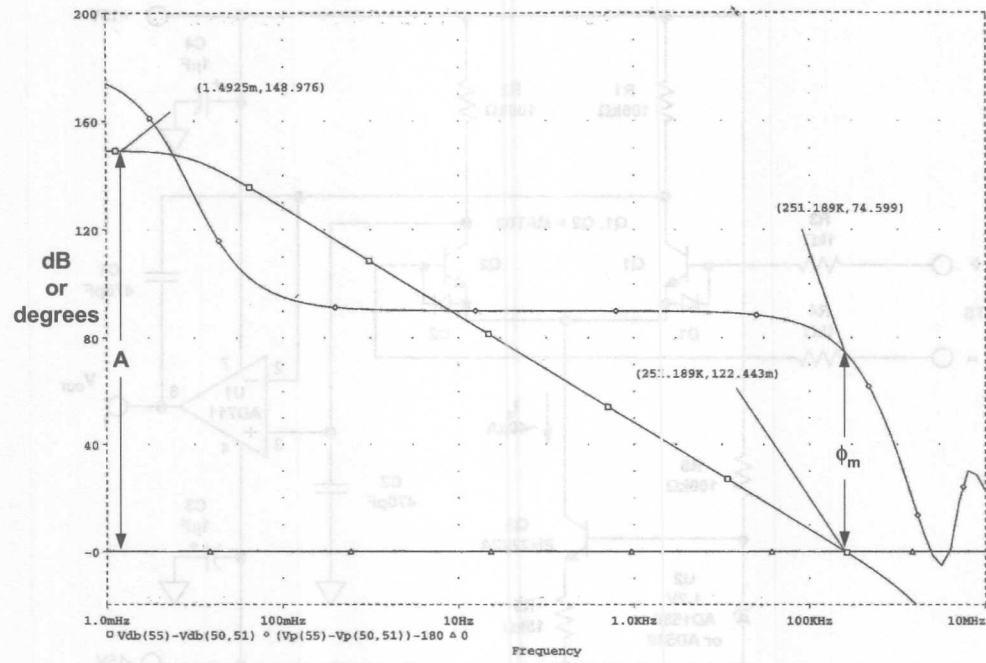
BIPOLAR TRANSISTOR GAIN-BOOSTED INPUT COMPOSITE OP AMP



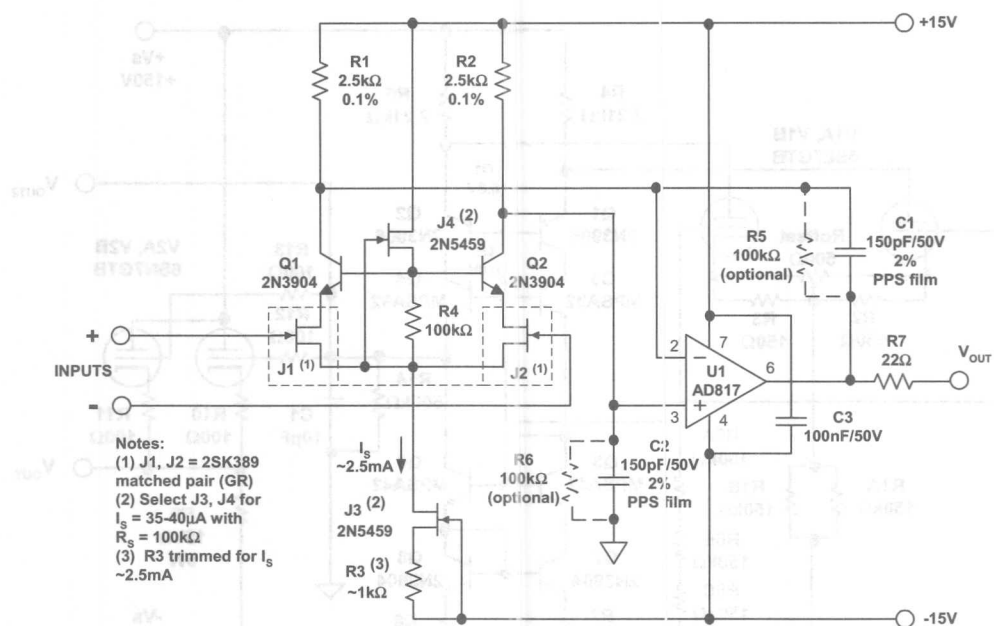
Op Amp Applications, Chapter 6

4.37

GAIN/PHASE VERSUS FREQUENCY FOR GAIN-BOOSTED INPUT COMPOSITE OP AMP



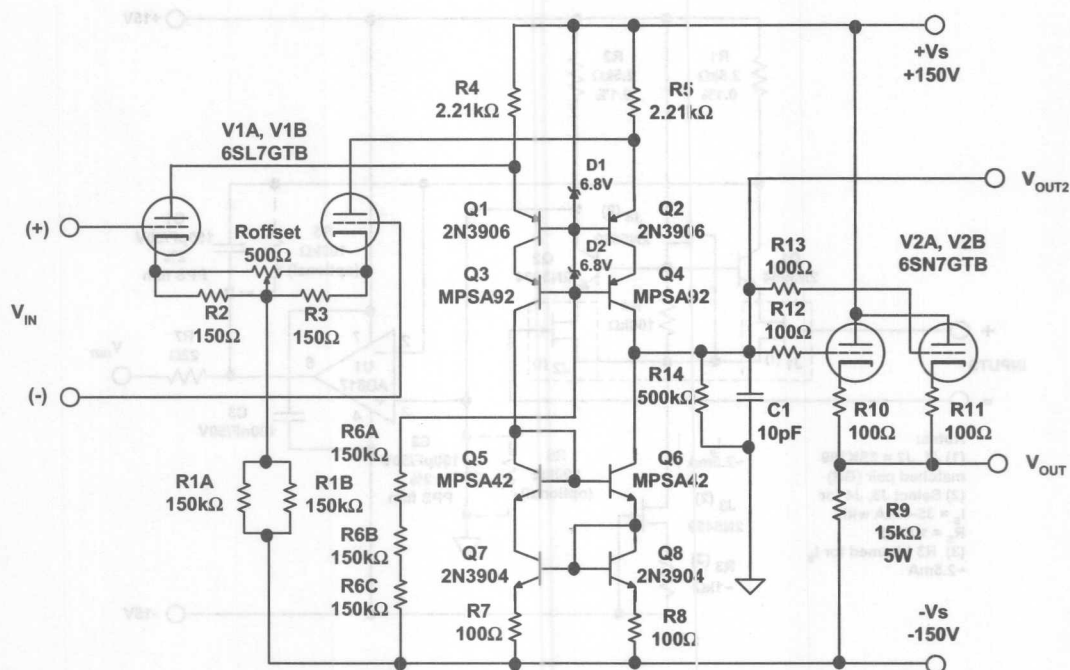
LOW NOISE JFET GAIN-BOOSTED INPUT COMPOSITE AMPLIFIER



Op Amp Applications, Chapter 6

4.39

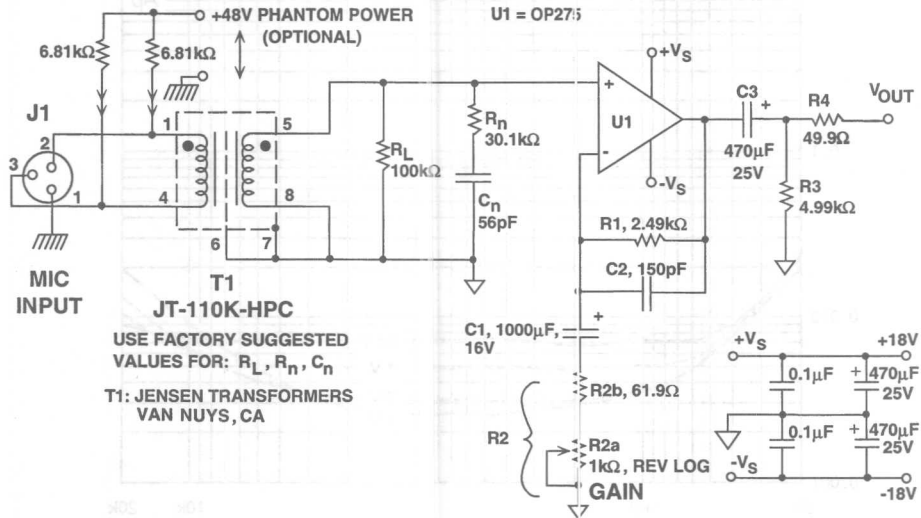
"NOSTALGIA" VACUUM TUBE INPUT/OUTPUT COMPOSITE OP AMP



Op Amp Applications, Chapter 6

4.40

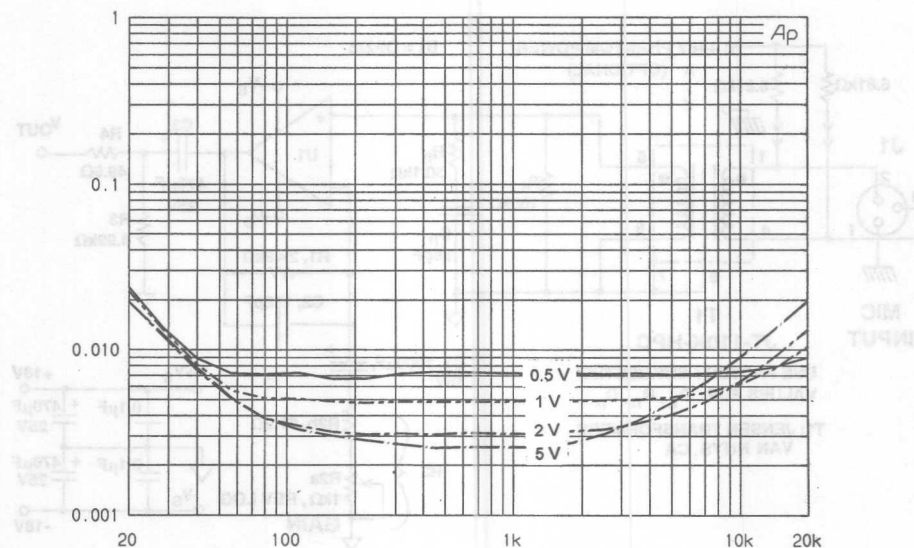
TRANSFORMER INPUT MIC PREAMPLIFIER WITH 28 TO 50 dB GAIN



Op Amp Applications, Chapter 6

4.41

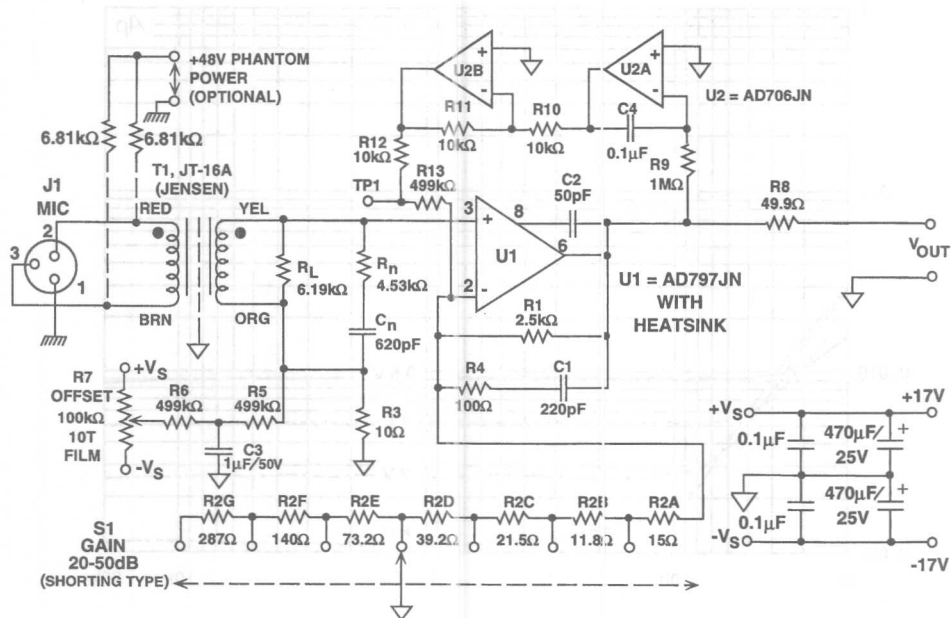
**TRANSFORMER COUPLED MIC PREAMPLIFIER THD+N (%) VERSUS
FREQUENCY (Hz) FOR 35dB GAIN, OUTPUTS OF 0.5, 1, 2, AND 5Vrms INTO 600Ω**



Op Amp Applications, Chapter 6

Op Amp Applications, Chapter 6 4.42

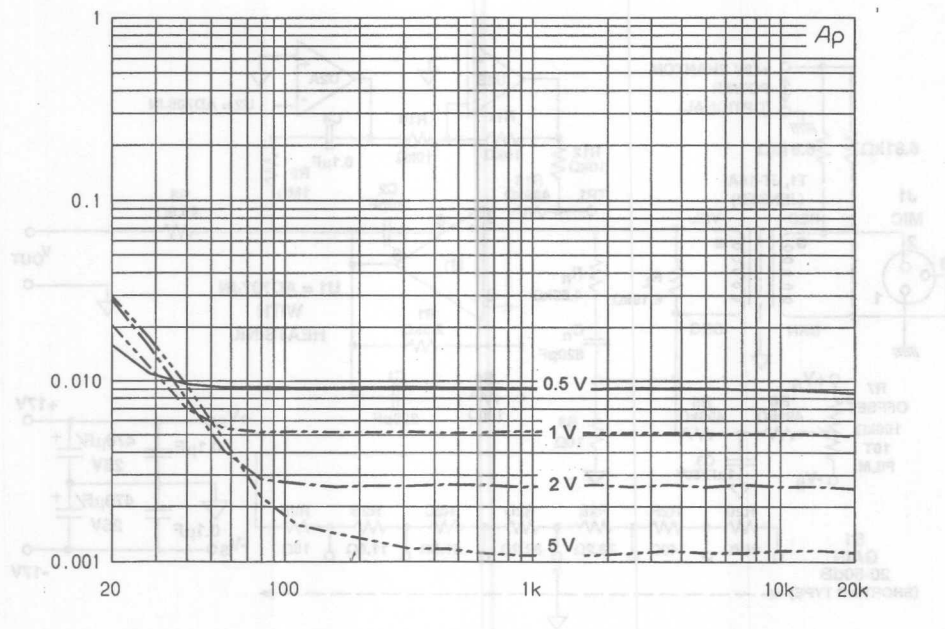
LOW NOISE TRANSFORMER INPUT 20 TO 50 dB GAIN MIC PREAMP



Op Amp Applications, Chapter 6

4.43

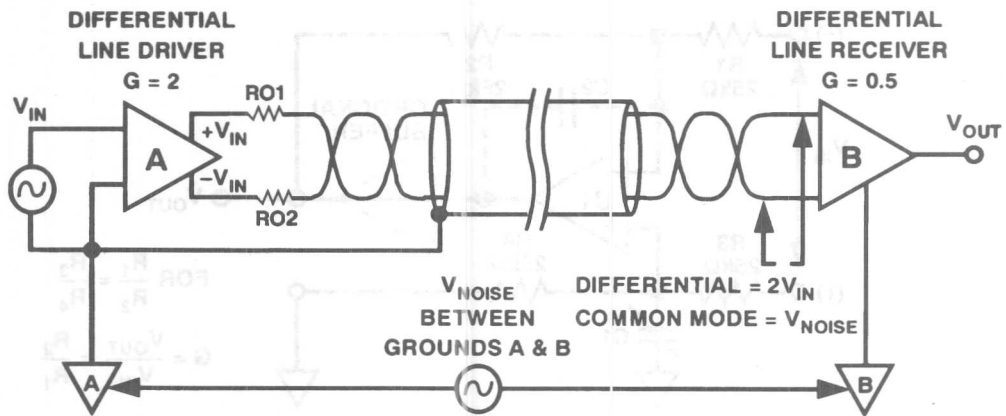
LOW NOISE TRANSFORMER INPUT MIC PREAMP THD+N (%) VERSUS
FREQUENCY (Hz) FOR 35dB GAIN, OUTPUTS OF 0.5, 1, 2, AND 5Vrms INTO 600Ω



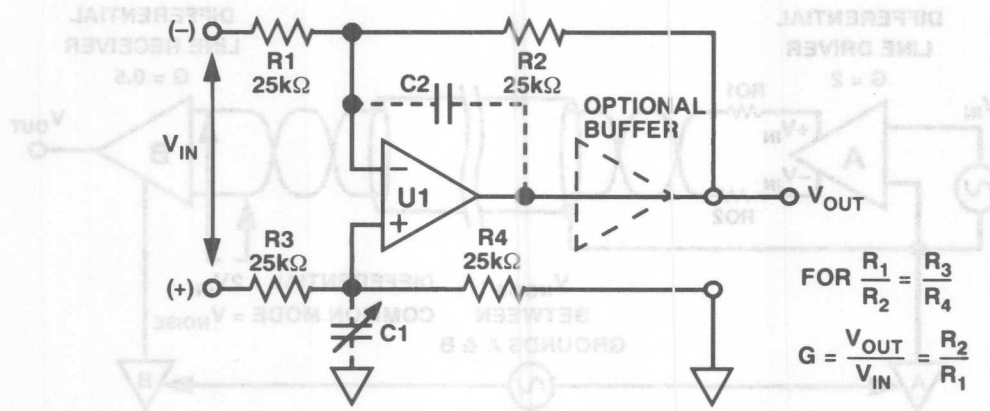
Op Amp Applications, Chapter 6

4.44

AN AUDIO BALANCED TRANSMISSION SYSTEM



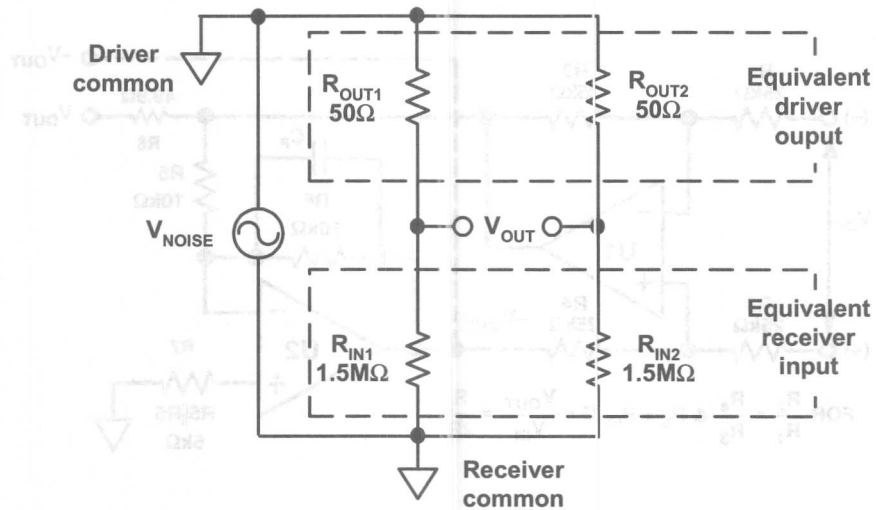
A SIMPLE LINE RECEIVER WITH OPTIONAL HF TRIM AND BUFFERED OUTPUT



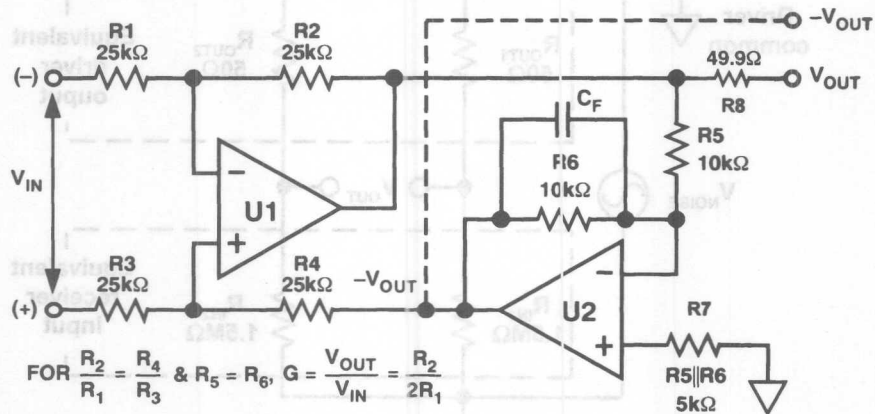
Op Amp Applications, Chapter 6

4.46

A CONCEPTUAL DRIVER/RECEIVER DIAGRAM OF A BALANCED LINE AUDIO SYSTEM WITH KEY IMPEDANCES AND CM NOISE



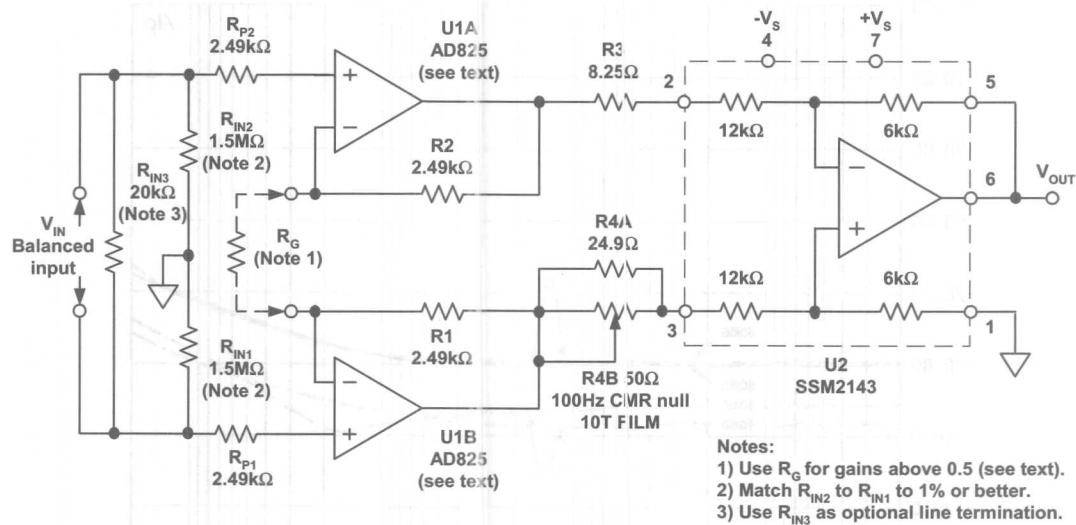
BALANCED LINE RECEIVER USING PUSH-PULL FEEDBACK



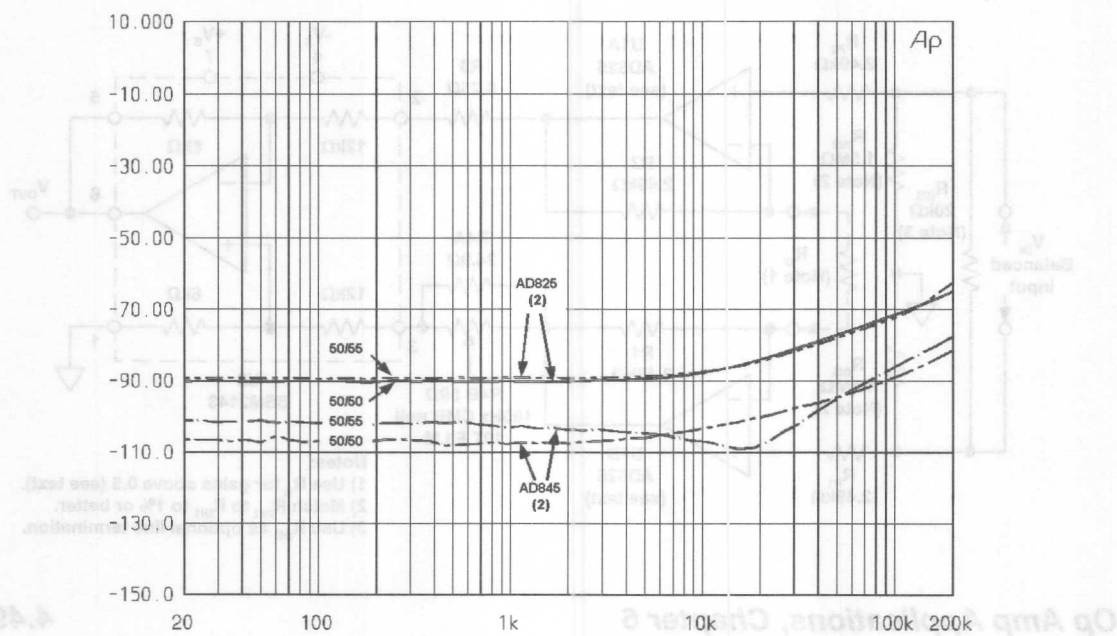
Op Amp Applications, Chapter 6

4.48

A BUFFERED INPUT BALANCED LINE RECEIVER



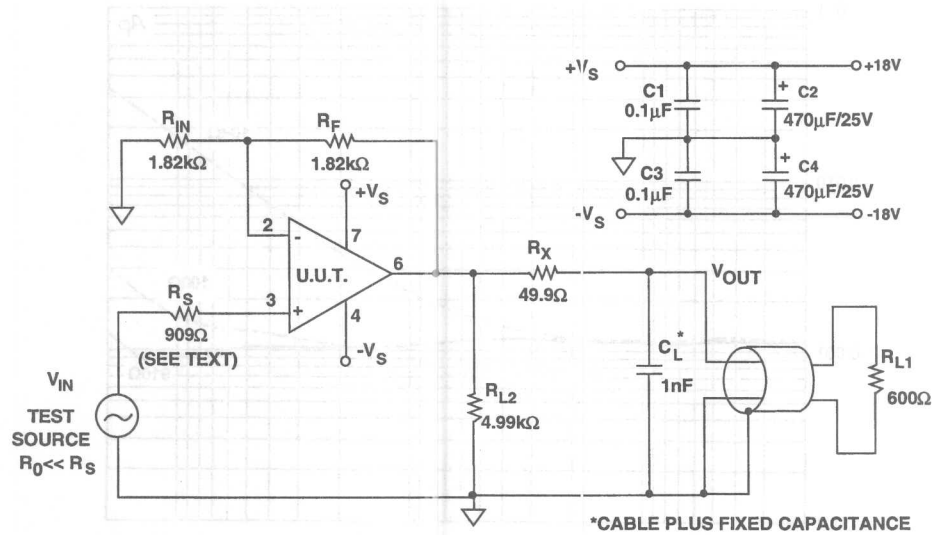
**CM ERROR (dB) VS. FREQUENCY (Hz), FOR AD325 AND AD845 PAIRS,
NOMINALLY 50Ω SOURCE IMPEDANCES MATCHED/MIS-MATCHED 10%**



Op Amp Applications, Chapter 6

4.50

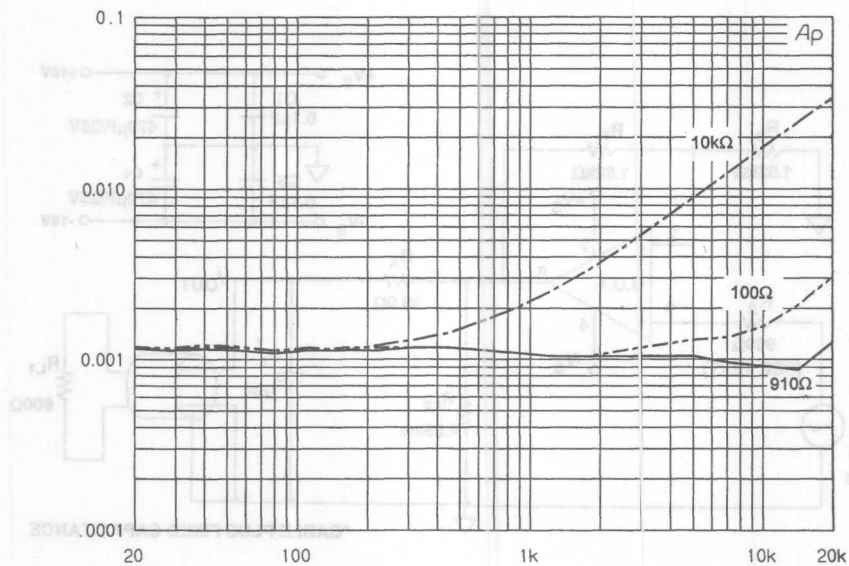
TEST CIRCUIT FOR AUDIO LINE DRIVER AMPLIFIERS



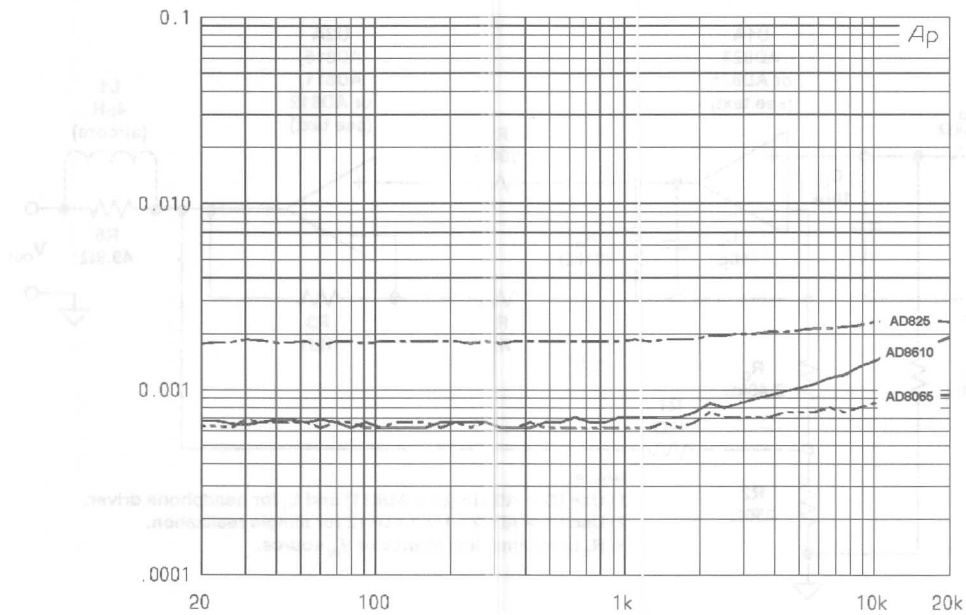
Op Amp Applications, Chapter 6

4.51

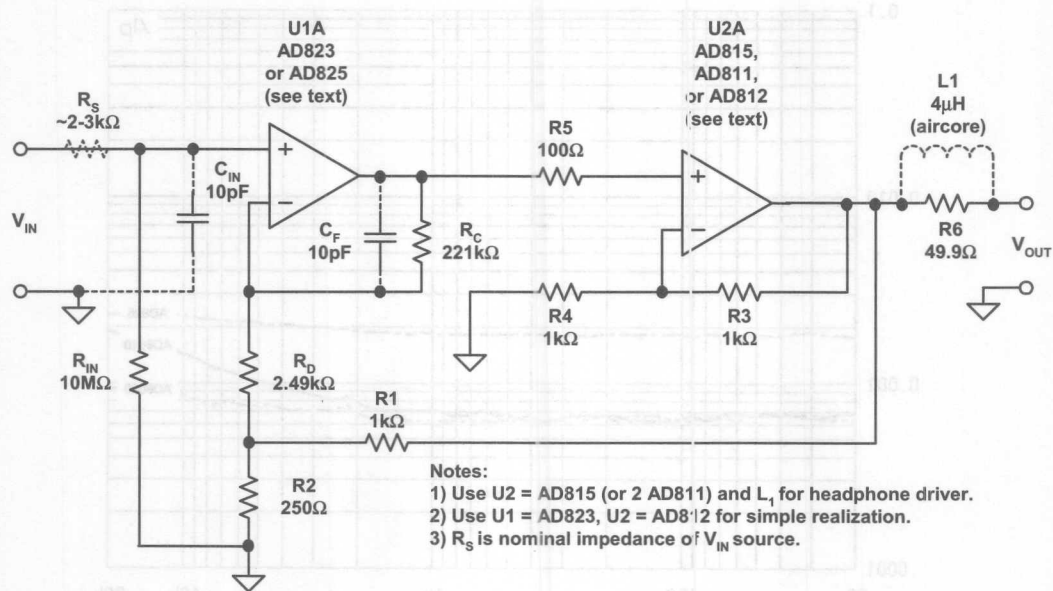
**FOLLOWER MODE R_S SENSITIVITY OF OP275 BIPOLAR/JFET INPUT OP AMP-
THD+N (%) VS. FREQUENCY (Hz), $V_{OUT} = 7V_{rms}$, $R_L = 500\Omega$, $V_S = \pm 18V$**



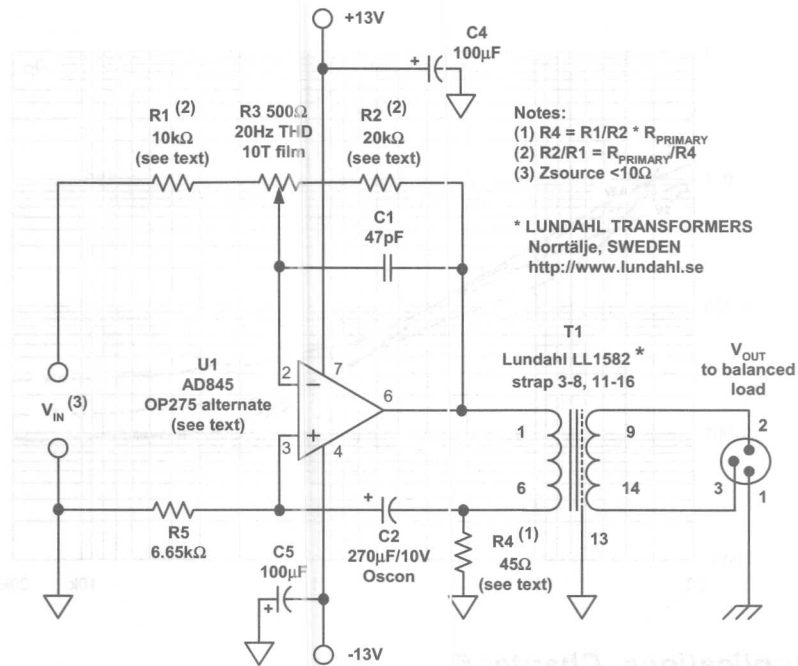
**C DRIVER GROUP, THD+N (%) VS. FREQUENCY (Hz), FOR
 $V_{OUT} = 7V_{rms}$, $R_S = 909\Omega$, $R_L = 500\Omega$, $V_S = \pm 13V$ OR $\pm 18V$**



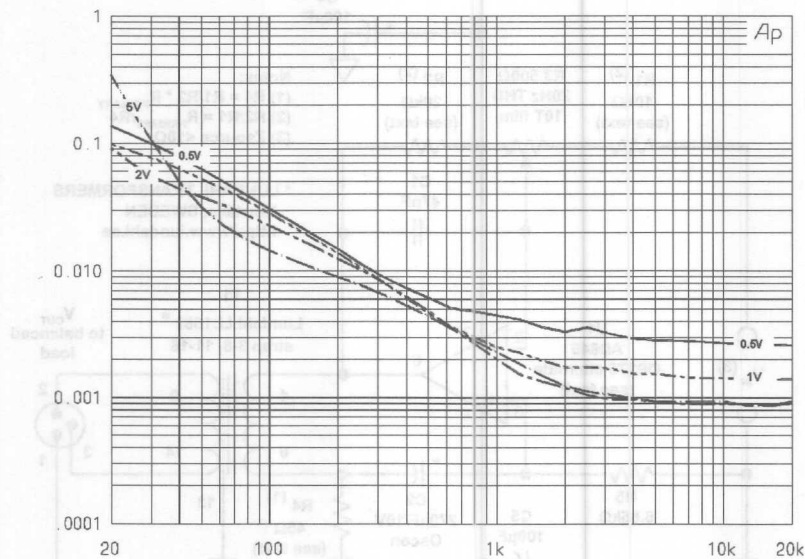
COMPOSITE CURRENT BOOSTED LINE DRIVER TWO



A BASIC SINGLE-ENDED MIXED FEEDBACK TRANSFORMER DRIVER



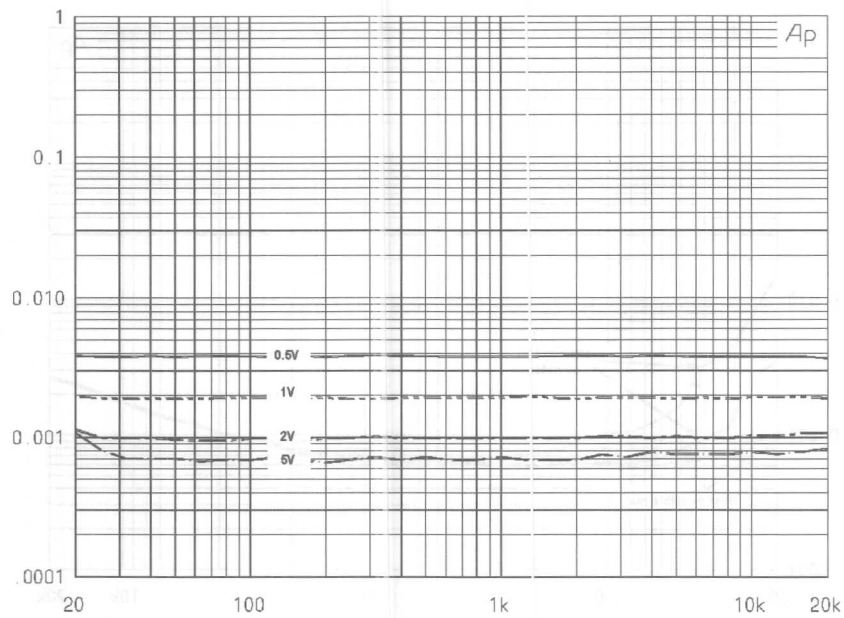
**LUNDAHL LL1517 TRANSFORMER AND DRIVER (WITHOUT FEEDBACK), THD+N
(%) VS. FREQUENCY (Hz), FOR $V_{OUT} = 0.5, 1, 2, 5V_{rms}$, $R_L = 600\Omega$**



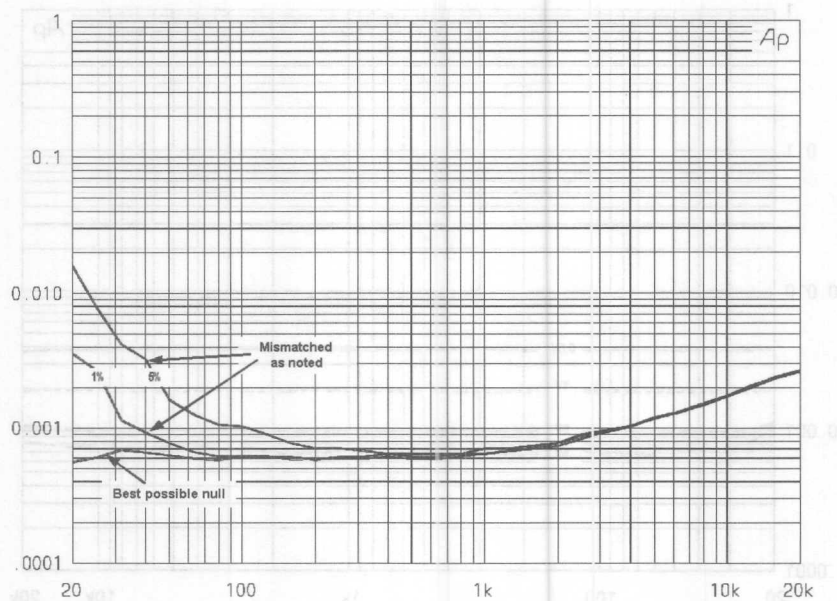
Op Amp Applications, Chapter 6

4.56

FIG. 6-61 DRIVER WITH LUNDAHL LL2811 TRANSFORMER AND AD845, THD+N (%) VS. FREQUENCY (Hz), FOR $V_{OUT} = 0.5, 1, 2, 5V_{rms}$, $R_L = 600\Omega$



**LUNDAHL LL1517 TRANSFORMER WITH MIXED FEEDBACK AD8610 DRIVER,
THD+N (%) VS. FREQUENCY (Hz) FOR VARIOUS NULL ACCURACIES**



Op Amp Applications, Chapter 6

4.58

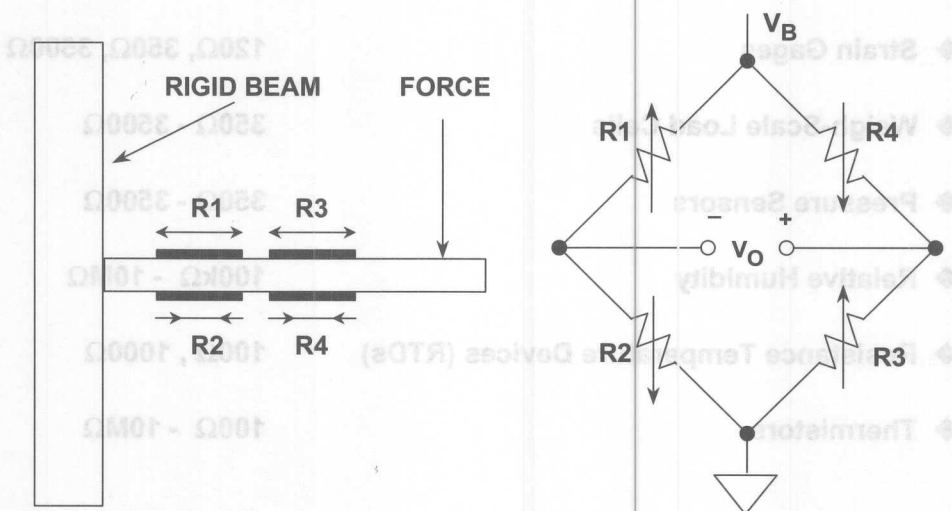
SENSOR RESISTANCES USED IN BRIDGE CIRCUITS SPAN A WIDE DYNAMIC RANGE

◆ Strain Gages	120 Ω , 350 Ω , 3500 Ω
◆ Weigh-Scale Load Cells	350 Ω - 3500 Ω
◆ Pressure Sensors	350 Ω - 3500 Ω
◆ Relative Humidity	100k Ω - 10M Ω
◆ Resistance Temperature Devices (RTDs)	100 Ω , 1000 Ω
◆ Thermistors	100 Ω - 10M Ω

Op Amp Applications, Chapter 4

4.59

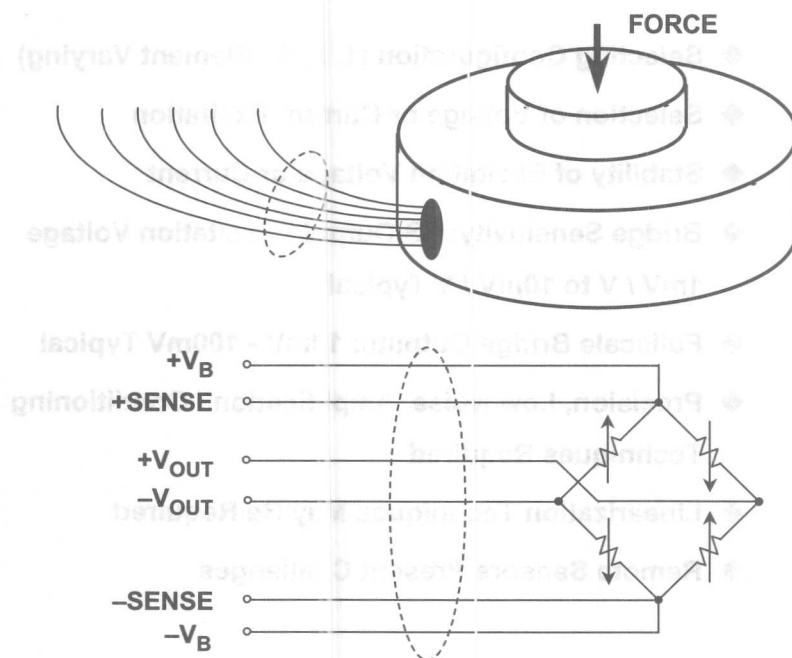
A BEAM FORCE SENSOR USING A STRAIN GAGE BRIDGE



Op Amp Applications, Chapter 4

4.60

A LOAD CELL COMPRISED OF 4 STRAIN GAGES IS SHOWN IN PHYSICAL (TOP) AND ELECTRICAL (BOTTOM) REPRESENTATIONS



Op Amp Applications, Chapter 4

4.61

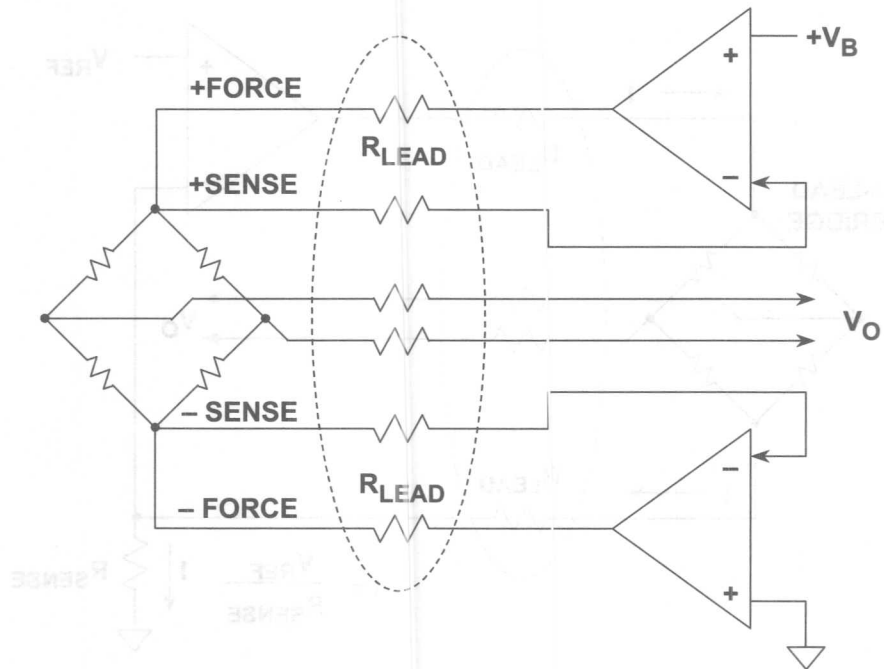
A NUMBER OF BRIDGE CONSIDERATIONS IMPACT DESIGN CHOICES

- ◆ Selecting Configuration (1, 2, 4 - Element Varying)
- ◆ Selection of Voltage or Current Excitation
- ◆ Stability of Excitation Voltage or Current
- ◆ Bridge Sensitivity: FS Output / Excitation Voltage
1mV / V to 10mV / V Typical
- ◆ Fullscale Bridge Outputs: 10mV - 100mV Typical
- ◆ Precision, Low Noise Amplification / Conditioning
Techniques Required
- ◆ Linearization Techniques May Be Required
- ◆ Remote Sensors Present Challenges

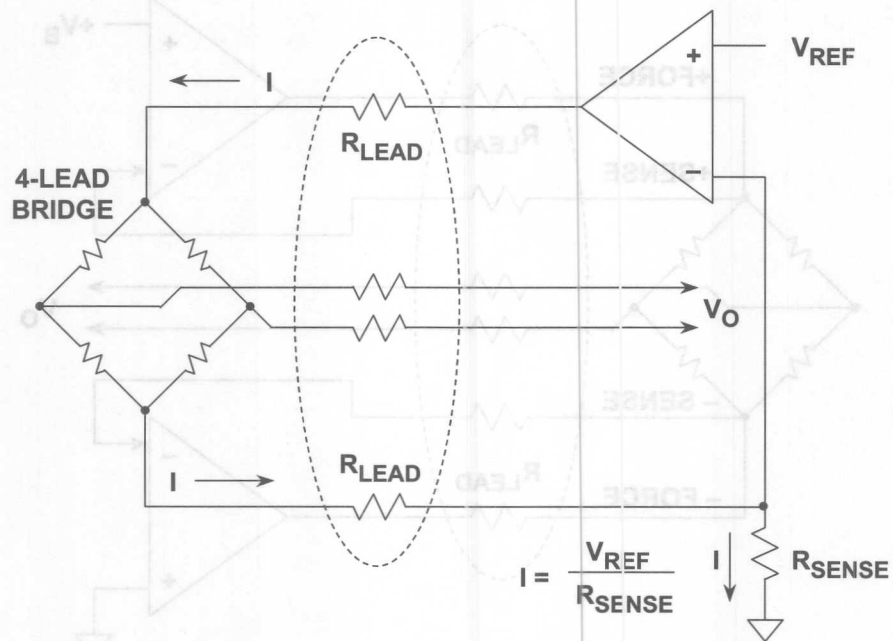
Op Amp Applications, Chapter 4

4.62

**KELVIN SENSING SYSTEM WITH A 6-WIRE VOLTAGE-DRIVEN
BRIDGE CONNECTION AND PRECISION OP AMPS MINIMIZES
ERRORS DUE TO WIRE LEAD RESISTANCE**



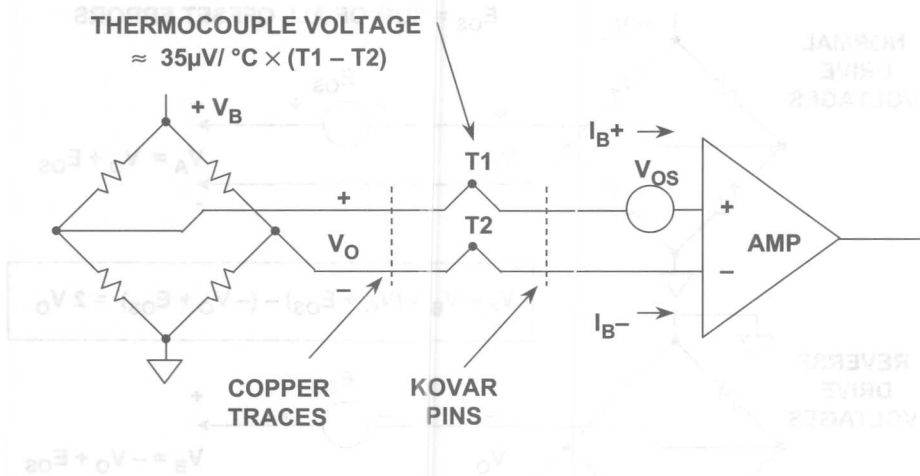
4-WIRE CURRENT-DRIVEN BRIDGE SCHEME ALSO MINIMIZES ERRORS DUE TO WIRE LEAD RESISTANCES, PLUS ALLOWS SIMPLER CABLING



Op Amp Applications, Chapter 4

4.64

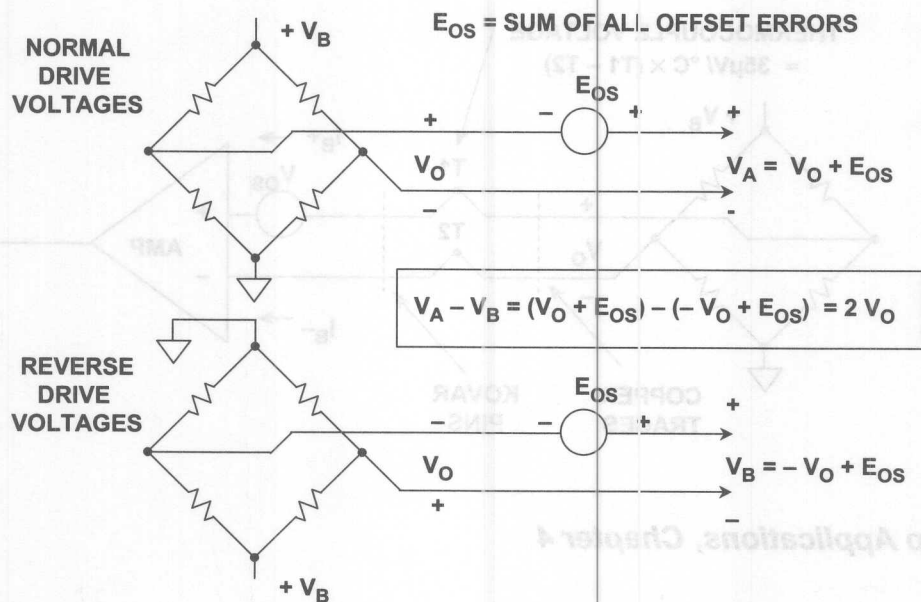
TYPICAL SOURCES OF OFFSET VOLTAGE WITHIN BRIDGE MEASUREMENT SYSTEMS



Op Amp Applications, Chapter 4

4.65

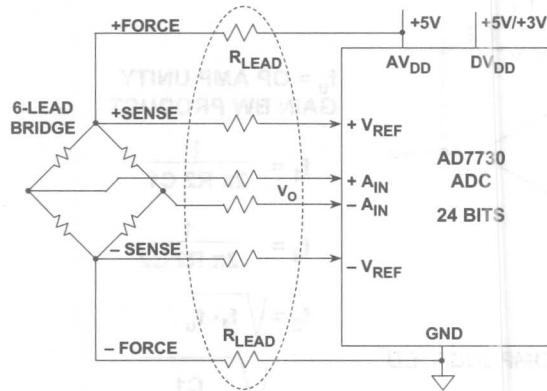
AC BRIDGE EXCITATION MINIMIZES SYSTEM OFFSET VOLTAGES



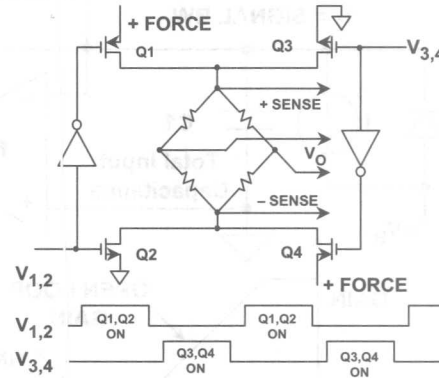
Op Amp Applications, Chapter 4

4.66

RATIOMETRIC DC OR AC OPERATION WITH KELVIN SENSING CAN BE IMPLEMENTED USING THE AD7730 ADC



(A) DC excitation

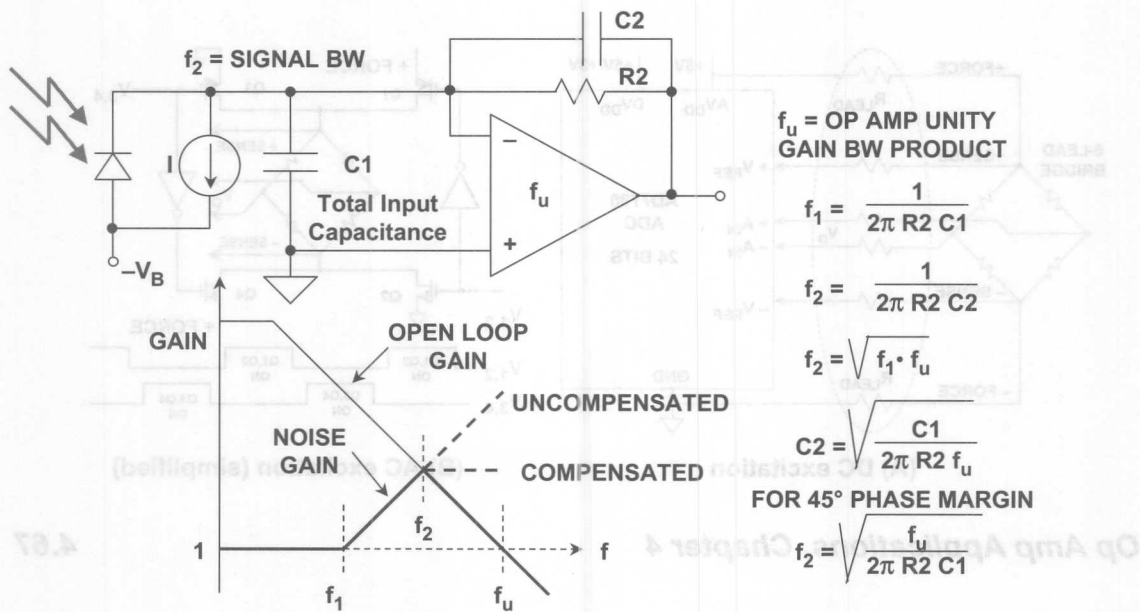


(B) AC excitation (simplified)

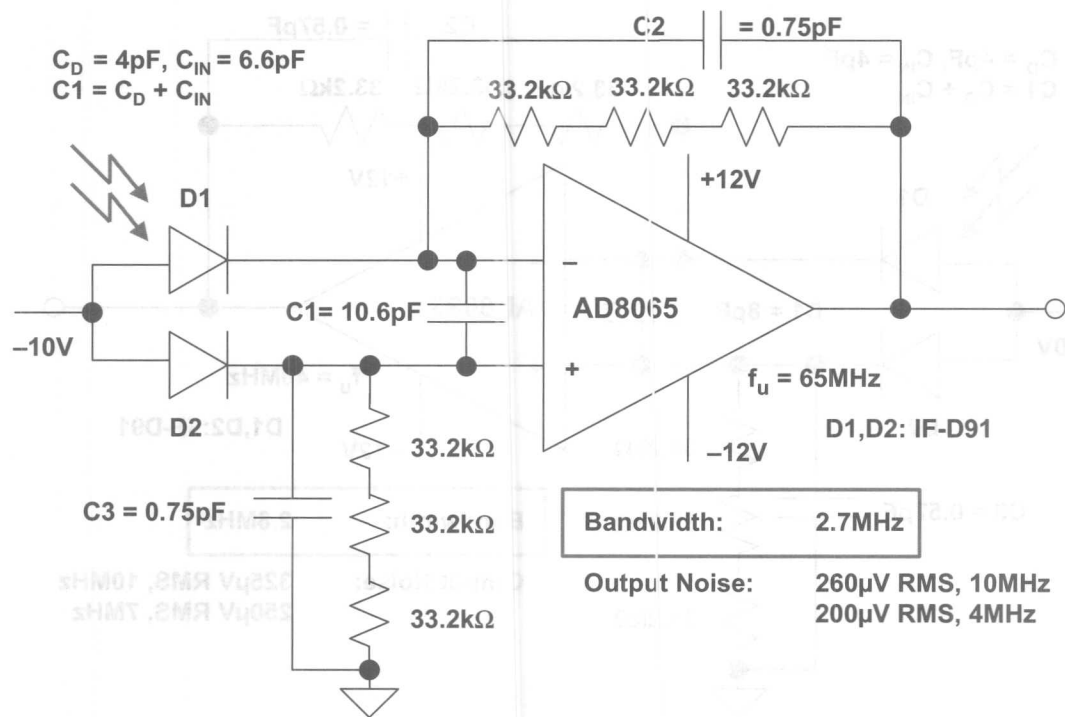
Op Amp Applications, Chapter 4

4.67

GENERALIZED MODEL FOR HIGH SPEED PHOTODIODE PREAMP

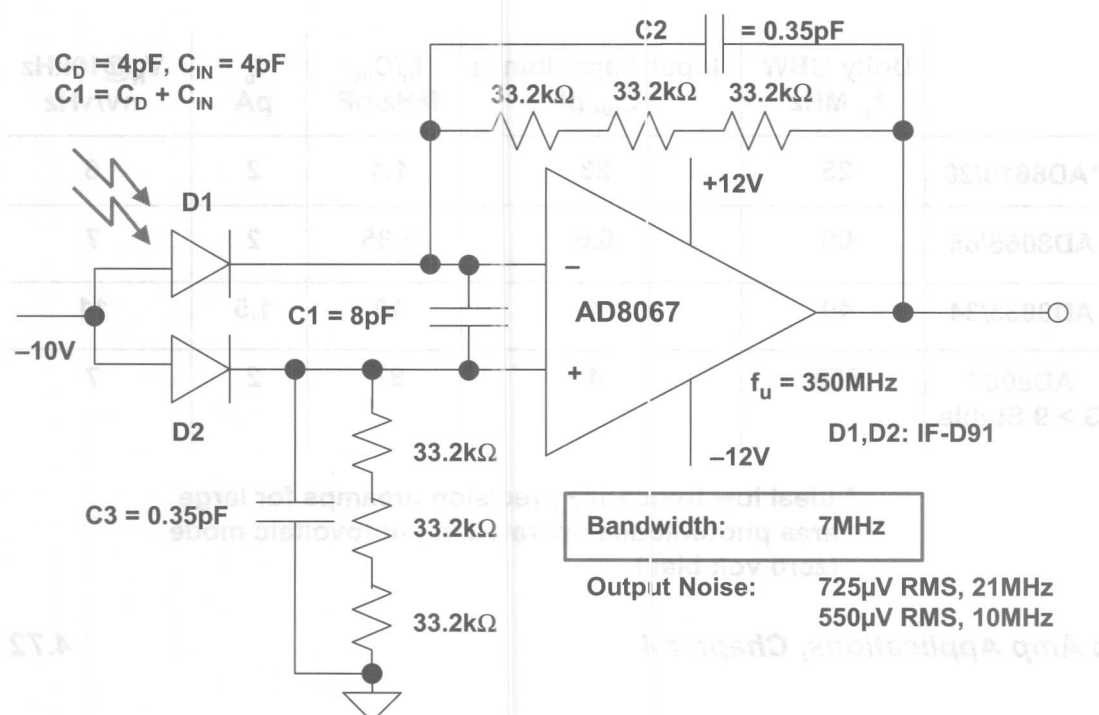


PHOTODIODE PREAMP USING THE AD8065



4.70

PHOTODIODE PREAMP USING THE AD8067



Op Amp Applications, Chapter 4

4.71

COMPARISON OF OP AMPS FOR PHOTODIODE PREAMPS

	Unity GBW f_u , MHz	Input Capacitance C_{IN} , pF	f_u/C_{IN} MHz/pF	I_b pA	$V_N@10kHz$ nV/ \sqrt{Hz}
*AD8610/20	25	23	1.1	2	6
AD8065/66	65	6.6	9.85	2	7
AD8033/34	40	4	10	1.5	11
AD8067 G > 9 Stable	350	4	87	2	7

* Ideal low frequency precision preamps for large area photodiodes operated in photovoltaic mode (zero volt bias)

Op Amp Applications, Chapter 4

4.72



Precision Single Supply Amps Selection Guide

Generic Part #				Supply Voltage		Rail-to-Rail		GBP (MHz)	I _{SY} (mA)	Packages*			Price† 1k
	1×	2×	4×	Min	Max	In	Out			SOT23	MSOP	TSSOP	
Communications													
AD	8541	8542	8544	+2.7	+5	x	x	1	0.055	x	x	x	---
AD	8565	8566	8567	+4.5	+16	x	x	4	0.85	x	x	x	---
AD	8531	8532	8534	+2.7	+5	x	x	3	1.25	x	x	x	---
AD	8591	8592	8594	+2.7	+5	x	x	3	1.25	x	x	x	---
AD	8601	8602	8604	+2.7	+5	x	x	8	1	x	x	x	---
AD	8605	8606	8608	+2.7	+5	x	x	10	1.2	x	x	x	---
SSM	2211			+2.7	+5		x	4	9.5				---
back to top													
Generic Part #				Supply Voltage		Rail-to-Rail		GBP (MHz)	V _{OS} (μV)	I _{BIAS} (nA)	e _{noise} (nV/√Hz)	Slew (V/μs)	Price† 1k
	1×	2×	4×	Min	Max	In	Out						
Industrial													
AD	705	706	704	±2	±18			.8	90	0.15	15	.15	---
AD	711	712	713	±4.5	±18			4	250	0.025	22	20	---
AD	795			±5	±18			1.6	250	0.002	11	1	---
AD	797			±5	±18			30	40	900	.09	20	---
AD	820	822	824	+3.0	±18		x	1.8	400	0.03	15	3	---
AD	8510	8512	8513	±5	±15			8	500	0.03	8	20	---
AD	8519	8529		±2.7	±12		x	8	1100	300	10	2.9	---
AD	8551	8552	8554	+2.7	+5	x	x	1.5	5	0.05	42	0.5	---
AD	8551	8552	8554	+4.5	+16	x	x	4	10mV	600	25	6	---
AD	8571	8572	8574	+2.7	+5	x	x	1.5	5	0.05	45	0.5	---
AD	8601	8602	8604	±2.7	±5	x	x	8	500	.06	33	5.2	---
AD	8605	8606	8608	±2.7	±5	x	x	10	300	.06	8	5	---
AD	8614		8644	5	±9	x	x	5.5	2500	400	12	7.5	---
AD	8601			±2.7	±5	x	x	2.2	5	0.1	22	0.8	---
OP	27			±4	±18			8	25	40	3	2.8	---
OP		270	470	±4.5	±18			5	75	20	3.2	2.8	---
OP		271	471	±4.5	±18			5	200	20	7.6	8.5	---
OP	97	297	497	±2	±20			1	25	.05	17	0.2	---
OP	113	213	413	±5	±15			3.5	125	600	4.7	0.9	---
OP	162	262	462	±3.0	±12		x	15	325	600	9.5	13	---
OP	184	284	484	±3.0	±15	x	x	3.25	65	350	3.9	2.4	---
OP	196	296	496	±3.0	±12	x	x	0.35	300	10	26	0.3	---
OP		249		±4.5	±18			4.7	300	.05	17	22	---
OP	777	727	747	±2.7	±30, ±15		x	0.7	100	11	15	0.2	---
OP	1177	2177	4177	±2.5	±18			1.3	60	2	8	0.7	---

* SOIC packages also available

** With V_{SY}=+5V

back to top													
Generic Part #		Supply Voltage		Rail-to-Rail		I _{OUT} (mA)	GBP (MHz)	Killer Applications	Price† 1k				
		Min	Max	In	Out								
Computer													
AD8614/44		+2.7	+16	x	x	100	5.5	LCD driver VCOM buffers	---				
AD8565/66/67		+4.5	+16	x	x	35	6	LCD driver greyscale op buffers	---				
AD8568/69/70		+4.5	+16	x	x	35	6	LCD driver greyscale op buffers	---				
OP162/262/462		+2.7	+12		x	30	15	LCD driver greyscale op buffers	---				
AD8532		+2.7	+5	x	x	250	3	Headphone amplifier	---				
AD8592		+2.7	+5	x	x	250	3	Headphone amplifier with shutdown	---				
SSM2211		+2.7	+5		x	350	4	Delivers 1W into a Mono 8Ω speaker	---				
SSM2250		+2.8	+5		x	350	4	Delivers 1W into a Mono 8Ω speaker, Drives Stereo Headphones	---				
back to top													
Generic Part #				Supply Voltage		Rail-to-Rail		I _{SY} (μA)	GBP (MHz)	Packages*			Price† 1k
	1×	2×	4×	Min	Max	In	Out			SOT23	MSOP	TSSOP	
Portable and Low Power													
AD	8517	8527		+1.8	+6	x	x	1200	7	x	x		\$0.85
AD	8541	8542	8544	+2.7	+5	x	x	55	1	x	x	x	\$0.61
AD	8591	8592	8594	+2.7	+5	x	x	1250	3	x	x	x	\$1.01
AD	8601	8602	8604	+2.7	+5	x	x	1000	8	x	x	x	---
AD	8605	8606	8608	+2.7	+5	x	x	1200	10	x	x	x	---
AD	8628			+2.7	+5	x	x	1400	2.2	x			---
AD	8631	8632		+1.8	+6	x	x	325	4	x	X		---
OP	191	291		+2	+15			20	.035				---
OP	196	296	496	+3.0	+12	x	x	60	0.35			x	\$1.18
OP	777	727	747	+2.7	+15		x	270	0.7		X	x	---
back to top													
Part Number		# per Device	Supply Voltage		Output		t _p (ns)	Max Freq (MHz)	I _{SY} (mA)	V _{CM} (V)**		Price 1k	
			Min	Max	TTL	CMOS				LOW	HIGH		
Comparators													
AD8561/64		1,4	+3.0	+12	x	x	7	60	5/14	0	3	\$1.58	
AD8511/12		1,2	+2.7	+5	x	x	4	100	10/20	0	3	---	
back to top													
Generic Part #	# per Device	Supply Voltage		Rail-to-Rail		GBP (MHz)	THD+N (dB)	e _{noise} (nV/√Hz)	Slew (V/μs)	Killer Applications	Price 1k		
		Min	Max	In	Out								
Audio													
OP275	2	+9	±18			9	115	6	22	Professional audio equipment	\$1.08		
SSM2135	2	+5	±15			3.5	105	5	1	DVD and CD players	\$1.78		
SSM2167	1	+1.8	+5		x	1	90	18	2	Mic pre-amp + compressor	---		
SSM2211	1	+2.7	+5		x	4	92	45	1	1W amplifier for 8Ω speaker	---		
SSM2250	2	+2.7	+5		x	4	92	45	1	Headphones + speaker	\$1.30		

* SOIC packages also available

** With V_{SY}=+5V

HIGH SPEED AMPLIFIER SELECTION GUIDE



	PART NUMBER				DISABLE	SUPPLY VOLTAGE					RAIL-TO-RAIL		MICRO PKG	A _{CL} MIN	BW @ A _{CL} [MHz]	SLEW RATE [V/μs]	DISTORTION SFDR ¹ @ BW FOR R _L			NOISE [nV/√Hz]	V _{OS} [mV MAX]	I _B [μA MAX]	I _{S/AMP} [mA TYP]	PRICE @ 1000 [OEM \$US]	
	SINGLES	DUALS	TRIPLES	QUADS		3 V	5 V	±5 V	±12 V	±15 V	IN	OUT					[dBc]	[MHz]	[Ω]						
DIFFERENTIAL	Drivers																								
	AD8131					●	●	●				●	2	400	2000	-77	20	800	13	5	6	8	1.80		
	AD8132					●	●	●				●	1	350	1200	-99	5	800	8	4	7	10.7	1.65		
	AD8138					●	●	●				●	1	310	1150	-94	5	800	5	3	5	20	3.75		
	Receivers																								
	AD8129					●		●	●	●			●	10	200	1100	-68	5	1k	4.5	1	3	11	1.55	
VOLTAGE FEEDBACK	AD8130					●		●	●	●			●	1	270	1100	-74	5	1k	12.5	2	3	11	1.55	
	Fast FET™																								
	AD8033 ³	AD8034				●		●	●	●		●	●	1	80	80	-81	1	1k	11	2	10 pA	3.3	1.19/1.59	
	AD8065	AD8066 ³						●	●	●		●	●	1	145	180	-88	1	1k	7	1.5	10 pA	6.4	1.59/2.19	
	AD8610	AD8620						●	●	●			●	1	25	50	-106 ²	0.02	600	6	0.25	10 pA	3	3.37/6.74	
	Low Cost, High Performance																								
	AD8038 ³	AD8039				●		●	●				●	1	350	425	-90	1	2k	8	3	0.75	1	0.85/1.20	
	AD8055	AD8056							●				●	1	300	1400	-85	5	1k	6	5	1	5	0.85/1.60	
	AD8057	AD8058				●	●	●					●	1	325	1150	-85 ²	5	1k	7	5	2	6	0.85/1.60	
	Rail-to-Rail																								
	AD8031	AD8032					2.7 V	●	●			●	●	●	1	80	32	-62 ²	1	1k	15	2	1.2	0.8	1.30/1.95
	AD8061/ AD8063	AD8062					2.7 V	8 V				●	●	●	1	300	800	-77	5	1k	8.5	6	10	6.8	0.85/1.60
	AD8091	AD8092					●		●			●	●	●	1	110	140	-75	5	2k	16	10	2.5	4.8	0.69/0.89
	Low Noise, Low Distortion																								
	AD8021					●		●	●	●			●	1	200	100	-92	1	1k	2.1	1	10	7	1.29	
		AD8022						●	●		●		●	1	75	100	-94	1	1k	2.5	5	2.5	3.5	2.35	
	AD9631							●	●					1	320	1300	-64	20	100	7	10	7	17	4.28	
	High Supply Voltage																								
AD817	AD826						●	●		●			1	50	350	-78	1	2k	15	2	6.6	7	1.58/2.18		
AD818	AD828						●	●		●			2	130	450	-78	1	2k	10	2	6.6	7	1.76/2.18		
CURRENT FEEDBACK	Low Cost																								
	AD8014						●	●				●	1	400	4000	-70	5	1k	3.5	5	15	1.1	1.19		
		AD8072	AD8073				●	●				●	1	200	500	-64	5	150	3	6	12	3.5	1.50/1.95		
	High Performance																								
	AD8001	AD8002						●				●	1	600	1200	-66	5	100	2	6	25	5	1.35/2.57		
				AD8004				●	●				1	250	3000	-78	5	1k	1.5	4	90	3.5	3.95		
	AD8005							●	●			●	1	270	1500	-53	5	1k	4	30	10	0.4	1.47		
	AD8007	AD8008 ³						●	●			●	1	650	1000	-83	20	150	2.7	4	8	9	1.19/1.99		
	AD8009							●	●			●	1	1000	5500	-54	100	100	1.9	7	150	14	1.59		
			AD8013			●		●	●				1	140	1000	-80	5	1k	3.5	5	15	4	4.38		
			AD8023			●		●	●				1	400	1200	-78	5	150	2	5	45	6.2	4.67		
	FIXED GAIN	Buffers																							
				AD8074			●		●					1	500	1400	-80	5	150	25	27	9	7.3	2.65	
			AD8075			●		●					2	450	1800	-74	5	150	25	40	10	8.3	2.65		
			AD8079					●					2	260	800	-78	5	1k	2	15	6	5	4.10		

¹Spurious Free Dynamic Range - Distortion @ Worst Harmonic ²THD - Total Harmonic Distortion ³Product Under Development

- June 2002

For more information on ADI High-Speed Amps visit our website at www.analog.com/highspeedamps



Generic Part Number	Supply Current	Operating Voltage Range	Gain Setting Method	CMRR @ 60 Hz, G=10	BW @ G=10	Settling Time to 0.01%, G=10	Input Voltage Offset	Input Voltage Offset TC	Input Bias Current	Output Offset Voltage	Input Voltage Noise Density (f=1 kHz)	Gain Range	Gain Error @ G=10	Price @ 100	Comments
	(mA) max	(V)		(dB) min	(kHz) typ	(μs) typ	(μV) max	(μV/°C) max	(nA) max	(mV) max	(nV/√Hz) max	min to max	(%) max	OEM \$US*	
In-Amps For New Designs Low Cost In-Amps															
AD622	1.3	±2.6 to ±18 Dual	Resistor	86	800	10	125	1	5	1.5	12 (typ)	1 to 1000	0.5	\$2.65	
AD623	0.55	±2.5 to ±6 Dual, +2.7 to +12 Single	Resistor	90	100	20	200	2	25	1	35 (typ)	1 to 1000	0.35	\$1.82	Lowest Cost In-Amp, μSOIC Packaging
AD8200	1	+4.7 to +12	Resistor	80	50	na	1000	15	na	1	300 (typ)	0.1 to 50	1	\$1.50	Lowest Cost Difference Amplifier
back to top															
In-Amps For New Designs Single Supply In-Amps															
AD623	0.550	±2.5 to ±6 Dual, +2.7 to +12 Single	Resistor	90	100	20	200	2	25	1	35 (typ)	1 to 1000	0.35	\$1.82	Lowest Cost In-Amp, μSOIC Packaging
AD626	2 0.29	±1.2 to ±6 Dual, +2.4 to +12 Single	Pin	66 (f=100 Hz)	100	24	500 2500	1 (typ)	ns	ns	250 (typ)	10, 100	0.5 1	\$3.69	Excellent for High Side Current Sensing
AD627	0.085	±1.1 to ±18 Dual, +2.2 to +36 Single	Resistor	77	80 (G=5)	135 (G=5)	200 250	3	10	1	38 (typ)	5 to 1000	0.35	\$2.71	Micro Power, Wide Supply Voltage Range
AD8200	1	+4.7 to +12	Resistor	80	50	na	1000	15	na	1	300 (typ)	0.1 to 50	1	\$1.50	Lowest Cost Difference Amplifier
back to top															
In-Amps For New Designs High Accuracy In-Amps															
AD620	1.3	±2.3 to ±18	Resistor	93	800	15	125	1	2	1	13	1 to 10,000	0.3	\$3.85	
AD621	1.3	±2.3 to ±18	Pin	93	800	12	250 (Total RTI)	2.5 (Total RTI)	2	na	17 (Total RTI)	10, 100	0.15	\$4.50	
back to top															
In-Amps For New Designs															

High Common-Mode Voltage Range

AD626	2 0.29	±1.2 to ±6 Dual, +2.4 to +12 Single	Pin	66 (f=100 Hz)	100	24	500 2500	1 (typ)	ns	ns	250 (typ)	10, 100	0.5 1	\$3.69	Excell High Current
AD629	1	±2.5 to ±18	na	77 (G=1)	500 (G=1)	15 (G=1)	1000 (Total RTI)	20	na	na	550 (Total RTO)	1	0.05 (G=1)	\$3.01	±250 \ CMV I
AD8200	1	+4.7 to +12	Resistor	80	50	na	1000	15	na	1	300 (typ)	0.1 to 50	1	\$1.50	Lowes Differ Amp

ba

In-Amps For New Designs Wide Bandwidth In-Amps

AMP03	3.5	±4.5 to ±18	na	80	3000	1 (typ)	ns	ns	ns	ns	750 (Total RTO)	1	0.008 (G=1)	\$3.03	
-------	-----	-------------	----	----	------	------------	----	----	----	----	--------------------	---	----------------	--------	--

ba

Vintage In-Amps High Accuracy In-Amps

AD524	5	±6 to ±18	Pin	90	400	15	250	2	±50	5	7	1 to 1000	±0.25	\$8.55	
AMP01	4.8	±4.5 to ±18	Resistor	95	100	13	100	1	6	6	59	0.1 to 10,000	0.8	\$10.18	

ba

Vintage In-Amps Low Noise In-Amps

AD624	5	±6 to ±18	Pin	90	1000 (G=1)	15	200	2	±50	5	4	1 to 1000	±0.05 (G=1)	\$14.98	
AD625	5	±6 to ±18	Resistor	90	400	15	200	2	±50	5	4 (Total RTI)	1 to 10,000	±0.05	\$12.58	

ba

Vintage In-Amps Software Programmable In-Amps

AD526	14	±4.5 to ±16.5	Software	ns	350 (G=16)	4.1 (G=16)	700	10	0.15	ns	30 (typ)	1,2,4,8,16	0.08 (G=16)	\$10.39	
-------	----	---------------	----------	----	---------------	---------------	-----	----	------	----	----------	------------	----------------	---------	--

Please note: an HTML version of this Selection Guide is available at <http://www.analog.com/technology/amplifiersLinear/designTools/selectionGuides/inamp.html>

